Timer Counter Series SM 201

Instruction Manual

SM201

MP MASTER
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Instruction Manual

TIMER/COUNTER

SERIES

SM 201

ISSUE 2

August 1972

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LIST OF AMENDMENTS

Al.No.	By Whom	Date	Al.No.	By Whom.	Date.

PREFACE

DAMAGE IN TRANSIT

Unpack the equipment and examine it thoroughly to ascertain whether any damage has occurred in transit. Report immediately any such damage to the agent or manufacturer. Retain the four rubberized packing surrounds, should a return to manufacturer be necessary.

GUARANTEE

2. All goods manufactured by the Company are guaranteed to the extent hereafter mentioned against defects arising from faulty material or workmanship subject to the goods not having suffered maltreatment or interference. The Company's liability under this guarantee is limited to replacing any part or parts found defective within a period as laid down in Company instructions after the date of delivery or installation.

If goods not of the Company's manufacture are ordered, the guarantee of that company is to be accepted.

LOCAL AGENTS ADDRESS:-

The address of your local agent is:-

DESCRIPTIVE MATTER AND ILLUSTRATIONS.

Descriptive matter, illustrations, dimensions and weights issued by the Company are typical and shall not be held as binding. The Company reserves the right to alter patterns and designs without notice.

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SECTION 1

SPECIFICATION

1. TIMER/COUNTER SM 201

Display: 6 side-view numerical indicator tubes with integral decimal points. Switchable (stored or non-stored).

Full Scale Count: 999999 plus overrange indication when full scale is exceeded.

A INPUT:

(i) Maximum Sensitivity: 10 mV r.m.s.

(ii) Input Impedance: 1 MΩ shunted with < 20 pF.

(iii) Maximum Amplitude: 300 V r.m.s. at 50 Hz.

(iv) Frequency Range: 10 Hz to 80 MHz at full sensitivity.
10 Hz to 100 MHz at 20mV r.m.s. (sinewave).
For pulse width limits see Section 3, Sub-section 8.

B INPUT and C INPUT:

(i) Sensitivity: Logic 1, > +1.2 V.
Logic 0, < +0.8 V.

(ii) Input Impedance: Logic 1, 1.5 kΩ in series with +1.2 V.
Logic 0, 30 kΩ in series with +5 V.

(iii) Maximum Amplitude: +15 V, −50 V.

(iv) Frequency Range: DC to 1 MHz.

NOTE: Contact closure is logic 0, contact open is logic 1.

External Clock Input (rear panel):

(i) Sensitivity: 0.5 V r.m.s. (sinewave)

(ii) Frequency Range: 1kHz to 10 MHz (sinewave)

(iii) Maximum Amplitude 70V r.m.s.

(iv) Input Impedance: 2.2 kΩ.

External Reset Input (rear panel): Sensitivity, Input Impedance and Maximum Amplitude as for B INPUT and C INPUT (above). Application of logic 0 activates reset.

Internal Clock Oscillator: 2 MHz crystal controlled oscillator with a temperature coefficient of less than 1 ppm/ ^{o}C, long term stability better than 20 ppm/annum.

Power Requirements:

(i) ***Voltage Range:*** 115 V +15% −20% ***or***, 230 V, +15% −20%.

(ii) ***Frequency Range:*** 45 Hz to 66 Hz.

(iii) ***Power Consumption:*** 25 VA approximately.

Operating Temperature Range: −10 °C to +50 °C.

Dimensions: (i) Front Panel: 33 cm (13 1/16 in.) x 8.9 cm (3 1/2 in.).

(ii) Depth: 29.2 cm (11 1/2 in.).

Weight: 5.7 kg (12 lbs) approximately.

2. TIMER/COUNTER SM 201/B

Specifications are as for model SM 201 but with a parallel BCD output on the rear panel:

(i) ***Logic 0:*** 0 V to +0.4 V, 10 mA sink capability.

(ii) ***Logic 1:*** +2.4 Vto +5 V, source resistance 1 kΩ.

BCD Outputs Unit SM 244: This kit comprises a BCD p.c. board and wired 34-way socket, which can be added to the basic instrument.

3. TIMER/COUNTER SM 201/H

Specifications as for model SM 201, but fitted with a clock oscillator of higher accuracy.

Internal Clock Oscillator:

Temperature Coefficient (average) over range, −10 °C to +50 °C:
2 parts in 10^9 per °C.

Long Term Stability:
< 1 part in 10^6 per annum

Daily Ageing Rate:
< 3 parts in 10^9 per day (average over 10 days)

SECTION 2

GENERAL INFORMATION

1. INTRODUCTION

1.1 Timer/Counter SM 201 is a portable instrument designed to operate over a frequency range of 10 Hz to 100 MHz. MSI integrated circuits are incorporated providing a very high reliability. Measurements are displayed on 6 side-view numerical indicator tubes with integral decimal points.

1.2 Sensitivity is controlled by a balanced attenuator that is switched by a four-position, front panel, rotary switch and can be selected to be 10 mV, 100 mV, 1 V or 10 V r.m.s. High noise rejection is a feature of the instrument, ensuring that it is not triggered in noisy environments. The sensitivity and level controls can be adjusted to ensure that the correct trigger point is selected.

1.3 Facilities to hold a reading indefinitely and to reset the instrument (manually or externally) are fitted and the display can be stored or non-stored as required. When the stored display is selected the reading is updated at the end of each counting sequence, presenting a non-blinking readout. With a non-stored display, the reading changes with each count made by the internal counting circuit, and thus is constantly changing. When the end of the counting sequence is reached the final reading is displayed until the start of the next counting sequence, when it is reset to zero.

1.4 An input voltage protection circuit is incorporated for input A and external clock input channels. the maximum safe input which can be applied is 300 V r.m.s. at 50 Hz for input A and 100 V r.m.s. at 50 Hz for the external clock input

1.5 Range selection is made by six push-button switches. Where a resolution in excess of full scale is required, the instrument can be used in the overrange condition. This is indicated by a front panel overrange lamp.

2. MODES OF OPERATION

2.1 The instrument has five modes of operation, which are selected by front panel mounted, push-button switches:

(a) ***Frequency Mode.*** In the frequency mode, the instrument measures the frequency of a signal applied to the A input , in terms of the internal clock oscillator, up to a maximum frequency of 100 MHz (typically 115 MHz). The accuracy is that of the clock oscillator ($\pm$ 1 count.) By operation of a front panel push-button, the instrument can measure frequency in terms of an externally connected clock oscillator, the frequency of which must lie within the limits 150 Hz to 10 MHz. A facility to hold a reading indefinitely is included by operation of a front panel push-button. This mode can also be used for ratio measurements.

(b) ***Period and Pulsewidth Modes.*** With the front panel toggle switch set to the period position, the instrument measures the period of a signal applied to the A input in terms of the internal clock oscillator. With the toggle switch set to the positive or negative pulsewidth positions, the corresponding pulse width is measured. An external clock oscillator can be used as in (a) above. Frequency and accuracy limitations are as for the Frequency mode. Time units are in seconds. This mode can also be used for ratio measurements.

(c) ***Average Period.*** In the Average Period mode, the instrument measures the average period of a signal applied to the the A input. The display indicates an average period measured over a series of periods up to 10^5 as determined by the range selectors. Time units are in microseconds. This mode can also be used for ratio measurements.

FIG. 2.1. TIMER/COUNTER SM 201

(d) ***Time Mode.*** In the Time mode, the instrument operates as an elapsed time meter with range selection as for the Period mode. The timing sequence is controlled by voltage transitions applied to the B input or B and C inputs, or manually by using the toggle switches on the front panel. Alternatively the timing sequence can be controlled by external remote contact closure operation. Closing the B input or C input to chassis is equivalent to a logic 1 to 0 transition on the input and similarly opening the contact is equivalent to a logic 0 to 1 transition.

(e) ***Count Mode.*** In the Count mode, the instrument counts the input signal applied to input A. The count is controlled in the same way as in the Time mode above.

22. Frequency ratio measurements can also be made by use of the external clock facility (although this is provided primarily to allow the instrument to operate from an external frequency standard). Measurements of frequency, period, average peric and time can be made relative to any externally connected frequency within the limits of the external clock input.

3. POWER REQUIREMENTS

3.1 The instrument is capable of operating from a power source in the range 115 V, +15% −20% or 230 V, +15%, −20% at frequencies between 45 Hz to 66 Hz. The power consumption is approximately 25 VA. The method of altering the instrume to suit the local power voltage is given in ***Section 3, Installation and Operation.***

4. PRINTER OUTPUT FACILITY

4.1 On Timer/Counter SM 201/B, a 50-way socket on the rear panel provides outputs suitable for driving a digital printer (such as SE LABORATORIES model type SM 250). Outputs available are, 6 decades of BCD plus overrange, a print command signal and a 0V (digital ground) line. This facility is also available in kit form (BCD Outputs Unit SM 244) that can be added to the standard Timer/Counter SM 201.

5. RACK MOUNTING KIT SM 210/R

5.1. The physical dimensions are such that the instrument can be used on the bench or rack mounted in standard 19 inch rack. The chassis is drilled to accept a rack mounting kit which is supplied as an optional extra.

SECTION 3

INSTALLATION AND OPERATION

1. INTRODUCTION

1.1 This section contains all the information necessary to install and operate the timer/counter.

2. UNPACKING

2.1 The instrument is supplied sealed in a polythene bag and is surrounded by rubber packing blocks. These should be retained for use again should further transportation be required.

3. EQUIPMENT LIST

3.1 The standard instrument is supplied with the following items:

(a) Miniature connectors, plug (for input A, B and C sockets), BNC type GE 35070/C 12 (Greenpar) pt. no. AS 0450.

(b) Fuse link, 200 mA, type TDC 123 (20 mm x 5 mm), fitted – pt. no. RS 23058.

(c) Terminal plugs for external clock and external reset inputs, type L 1716, Belling and Lee, pt. no. AS 0459 (red).

(d) Terminal plugs for earth connections, type L 1716, Belling and Lee, pt. no. AS 0460 (black).

(e) Printer plug, 34-way, McMurdo MP 134, pt. no. AS500, with locking plate, pt. no. AS 0426 and cover, pt. no. AS 50

(f) Instruction Manual.

(g) Carrying Case SM 210/C (optional at extra cost). (h) Rack Mounting kit SM 210/R (optional at extra cost).

The instrument has five modes of operation, which are selected by front panel mounted, push-button switches:

a) ***Frequency Mode.*** In the frequency mode, the instrument measures the frequency of a signal applied to the A input , in terms of the internal clock oscillator, up to a maximum frequency of 100 MHz (typically 115 MHz).

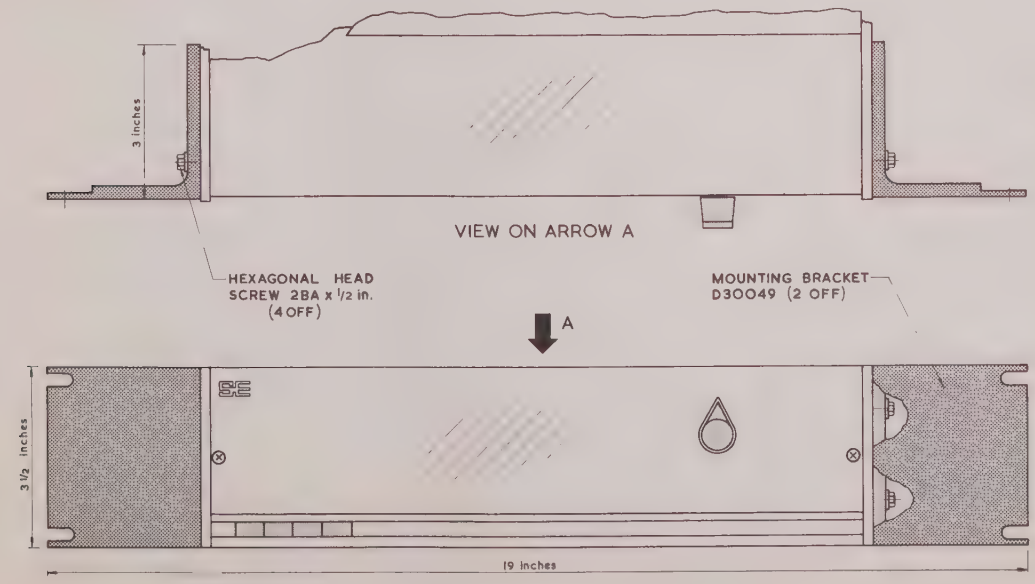
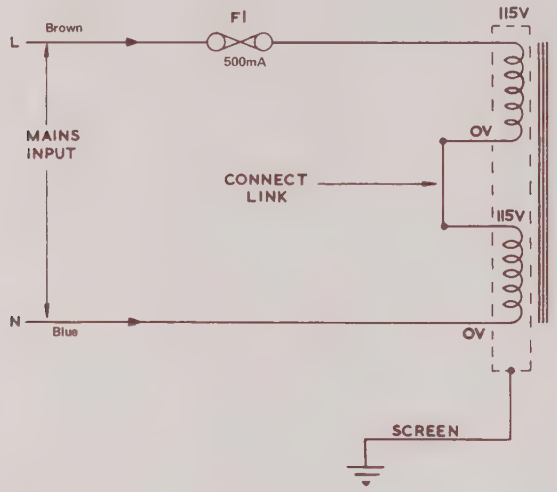


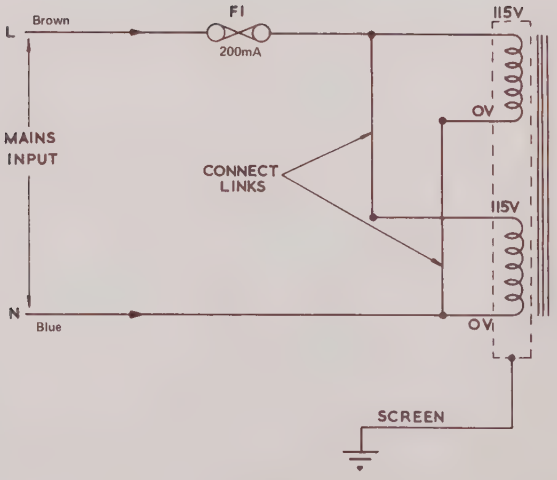
FIG. 3.1. RACK MOUNTING DETAILS

4. RACK MOUNTING

4.1. The SM 201 can be bench or rack mounted. Extensions are added to either side of the front panel so that it can be held in place in the rack. This system is available in kit form as an optional extra, and is shown in fig. 3.1.



CONNECTION FOR 230V MAINS INPUT



CONNECTION FOR 115V MAINS INPUT

FIG. 3.2. POWER SOURCE SELECTION

5. OPERATING POWER SOURCE

5.1. The timer/counter is supplied wired to accept the mains input voltage as specified by the customer. For 230 V operation, primary windings of T1 are connected in series, and for 115V operation, they are connected in parallel – See fig. 3.2. Unless specified, the instrument is connected for 230V.

CAUTION

Ensure that the instrument is isolated from the power source when changing the voltage tappings.

6. CONNECTIONS

6.1. Power Lead

6.1.1. The power lead should be connected: Brown wire to Live, Blue wire to Neutral and Green/Yellow wire to Earth (ground).

6.2. Printer Socket

6.2.1. The pin connections and functions for the (34-way) printer socket are listed below. The logic levels are:

Logic 1: +2.4 V min to +5 V max.

Logic 0: 0 to + 0.4 Vmax. sink capability10 mA.

(a) BCD Outputs:

Overrange Digit Pin No	100,000's Decade Pin Nos.	10,000's Decade Pin Nos.	1000's Decade Pin Nos.	100's Decade Pin Nos.	10's Decade Pin Nos.	Units Decade Pin Nos.	BCD Code
–	D6	D5	D4	D3	D2	D1	8
–	C6	C5	C4	C3	C2	C1	4
–	B6	B5	B4	B3	B2	B1	2
A7	A6	A5	A4	A3	A2	A1	1

(b) Print Command:

Pin No.	Logic State
C7	Logic 1 to command print.

(c) 0 V (digital ground): pin B7. The 0V is connected to power earth and chassis.

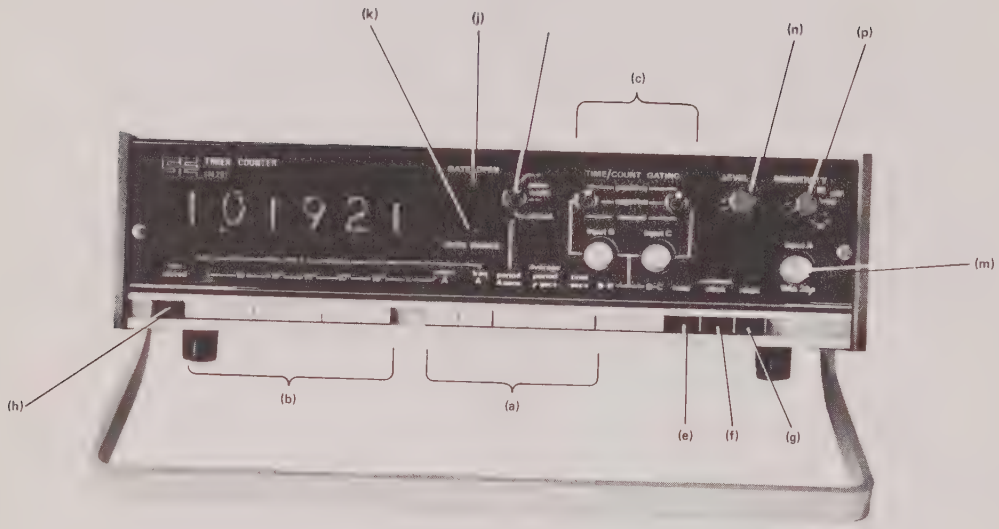
7. SUMMARY OF CONTROLS, CONNECTORS AND INDICATORS

7.1 The controls, connectors and indicators located on the front panel are summarized as follows (see fig. 3.3.):

(a) Mode Select Push-buttons:
(See (b) for ranges.)

(i) COUNT A: Selects Count mode.

(ii) FREQ A: Selects Frequency mode, readings displayed in MHz or kHz.



(a) MODE SELECT
(b) RANGE
(c) TIME/COUNT GATING
(d) PERIOD/PULSEWIDTH POLARITY
(e) HOLD
(f) EXTERNAL CLOCK SELECT
(g) RESET
(h) STORED/NON-STORED DISPLAY SELECTOR
(j) GATE OPEN INDICATOR
(k) OVERRANGE INDICATOR
(m) SIGNAL INPUT CONNECTOR
(n) LEVEL CONTROL
(p) SENSITIVITY CONTROL

FIG. 3.3. CONTROLS, CONNECTORS AND INDICATORS – FRONT PANEL

(c) TIME/COUNT Gating Controls:

(a) INPUT B Channel.

(i) ***B-B push-button:*** 'Start' and 'stop' for Time and Count modes gated from INPUT B signal.

(ii) ***INPUT B Connector:*** Gating signal for B channel connected here.

(iii) ***B POSITIVE: NEGATIVE: MANUAL Switch:*** Selects method of 'start:stop' facility.

(b) INPUT C Channel.

(i) ***B-C Push-button:*** 'Start' and 'stop' for Time and Count modes
'Start' on INPUT B signal.
'Stop' on INPUT C signal.

(ii) ***INPUT C Connector:*** Gating signal to stop Time and Count modes (in B and C gating) connected here.

(iii) ***C POSITIVE: NEGATIVE: MANUAL switch:*** Selects method of 'stop' facility.

(d) PERIOD: PULSEWIDTH + – Switch:

This switch is used in the single period mode:

(i) ***Period:*** The period of a signal on INPUT A is measured in seconds.

(ii) ***Pulsewidth +:*** The pulse width of a positive going pulse on INPUT A is measured in seconds.

(iii) ***Pulsewidth–:*** The pulsewidth of a negative going pulse on INPUT A is measured in seconds.

(e) HOLD Push-button:

This facility operates in any mode. When selected, inhibits automatic resetting of the instrument at the end of a measurement sequence, thus displaying the last measurement made (until the instrument is reset manually or by the external reset signal).

(f) EXTERNAL CLOCK Push-button:

When selected inhibits internal clock operation, so that the instrument can be driven from an external oscillator (150 Hz to 10 MHz). Can be used on all modes, except Count.

(g) RESET Push-button:

When depressed, it resets the display to zero. When released, the instrument can take further measurements as selected by other controls.

(h) NON-STORED push-button:

When selected, the display follows the main counter during the measurement sequence and holds the reading until the next reading is initiated. When the push-button is released (out), the instrument operates in the 'stored' mode and the display is updated at the end of each measurement sequence.

(j) GATE OPEN Indicator:

When lit, this lamp indicates that the instrument is taking a measurement. During unlit periods, the instrument is updating readings and resetting counting circuits ready for the start of the next count or sequence.

(iii) ***PERIOD A SECS:*** Selects Single Period mode to give readings in seconds. Used in conjunction with PERIOD: PULSEWIDTH switch (d).

(iv) ***AVERAGE PERIOD μSECS:*** Selects Average Period mode to give readings in microseconds.

(v) ***TIME SECS:*** Selects Time mode. Can be used with B-C gating. for alternative method of pulse width measurement. (See Para. 8.6.2)

(b) Range Switches:

(i) ***MHz/1:*** Selects range up to full scale readings of:

Frequency:	**9999.99 MHz** (max. freq. 115 MHz typical).
Period:	**0.999999 seconds**
Average Period:	**999999 μs**
Count :	**999999**
Time:	**0.999999 seconds**

(ii) **MHz/10:** Selects range up to full scale readings of:

Frequency:	**999.999 MHz** (max. freq. 115 MHz typical).
Period:	**9.99999 seconds**
Average Period:	**99999.9 μs**
Count:	**999999 x 10**
Time:	**9.99999 seconds**

(iii) ***MHz /10^2:*** Selects range up to full scale readings of:

Frequency:	**99.9999 MHz**
Period:	**99.9999 seconds**
Average Period:	**9999.99 μs**
Count:	**999999 x 10^2**
Time:	**99.9999 seconds**

(iv) ***kHz /10^3:*** Selects range up to full scale readings of:

Frequency:	**9999.99 kHz**
Period:	**999.999 seconds**
Average Period:	**999.999 μs**
Count:	**999999 x 10^3**
Time:	**999.999 seconds**

(v) ***kHz /10^4:*** Selects range up to full scale readings of:

Frequency:	**999.999 kHz**
Period:	**9999.99 seconds**
Average Period:	**99.9999 μs**
Count:	**999999 x 10^4**
Time:	**9999.99 seconds**

(vi) ***kHz/10^5:*** Selects range up to full scale readings of:

Frequency:	**99.9999 kHz**
Period:	**99999.9 seconds**
Average Period:	**9.99999 μs**
Count:	**999999 x 10^5**
Time:	**99999.9 seconds**

(k) OVER RANGE Indicator: When lit, this lamp indicates that the value of the reading to be displayed is higher than the capacity of the main counter. The instrument can be used in the 'overrange' condition to obtain a higher resolution than that given by the 6 significant digits available, provided that the non-displayed (most significant) digits are known, by first taking a measurement at a shorter gate time. This increases the effective resolution.

(m) INPUT A Connector: The 'signal to be measured' is connected here for all modes except Time mode.

(n) LEVEL Control: This control is adjusted in conjunction with the SENSITIVITY switch to obtain the correct trigger point on the'signal to be measured'.

(p) SENSITIVITY switch: Four-position switch, with the most sensitive position at the 10 mV r.m.s. range. Having selected the sensitivity, the LEVEL control is adjusted for correct trigger point if necessary.

7.2. Connectors and switches located on the rear panel are as follows (see Fig. 3.4.):

(a) POWER ON OFF Switch: At ON, the numerical indicator tubes glow.

(b) Printer Output Socket: Fitted to SM 201/B only and provides, 6 decades of BCD (8421) code output of each displayed reading together with overrange and print command. For connections and logic levels see Para 6.2.

(c) External Clock Input Sockets: These accept the output from an external clock oscillator, frequency limits 150 Hz to 10 MHz (sinewave).

(d) External Reset Input Sockets: These accept an external reset signal. Application of logic 0 activates reset ,(logic levels as BCD outputs).

8. OPERATING INSTRUCTIONS

The following procedures are correct assuming the internal clock oscillator is being employed. External clock operation and the use of the LEVEL and SENSITIVITY controls are described under separate headings. The effects of noise on incoming waveforms are dealt with under ***Application Notes.***

8.1. Preliminary Checks and Precautions

(a) If the instrument has been in store for a prolonged period , check for evidence of dampness before switching -on. If damp, dry out with warm, dry air.

(b) For normal use, the instrument should be grounded. However, if the mains frequency is to be measured it is important to ensure that excessive currents do not flow in the input low line. This can be done in one of two ways:—

(i) using an isolating transformer across the INPUT A connector.

(ii) resistively coupling the INPUT A high side to mains live (1MΩ) and selecting the highest range. No connection required to INPUT A low side.

8.2. Frequency Measurement

8.2.1. In this mode, the instrument measures the frequency of a signal applied to the front panel INPUT A connector in terms of its internal clock oscillator. The maximum sensitivity is 10mV r.m.s. Frequency limits are between 10Hz and 80MHz at full sensitivity and 10Hz to 100MHz at 20mV r.m.s. Minimum pulsewidth is 5nsecs.

(a) Connect the signal to be measured to INPUT A.

(b) Set the controls as follows:

(i) Select the FREQ A push-button

(ii) Check that NON-STORED push-button is not selected. For normal operation on the Frequency mode, the instrument is used with the 'stored-display' facility, the reason being that the period of stable display is very short, and with non-stored selected, the display would appear as a 'multi-glow' reading.

(iii) Ensure that the EXTERNAL CLOCK push-button is not selected.

(iv) Select the highest (frequency) range push-button (when the frequency is unknown) and then 'range-down' until sufficient resolution is obtained:

Range (left to right)	Gate Time	Full Scale Reading
1	100 µs	9999.99 MHz (see note)
2	1 ms	999.999 MHz (see note)
3	10 ms	99.9999 MHz
4	100 ms	9999.99 kHz
5	1 s	999.999 kHz
6	10 s	99.9999 kHz

NOTE: In FREQ A mode, the high frequency limit is 100 MHz, typically 115 MHz.

(v) Adjust the LEVEL and SENSITIVITY controls if necessary (see ***Application Notes***).

(c) To hold a reading, press the HOLD push-button. To obtain a new reading press and release the RESET push-button. Operation of the RESET push-button resets the counter circuit and display to zero. A new reading is initiated when the push-button is released.

8.3 Single Period and Pulsewidth Measurement

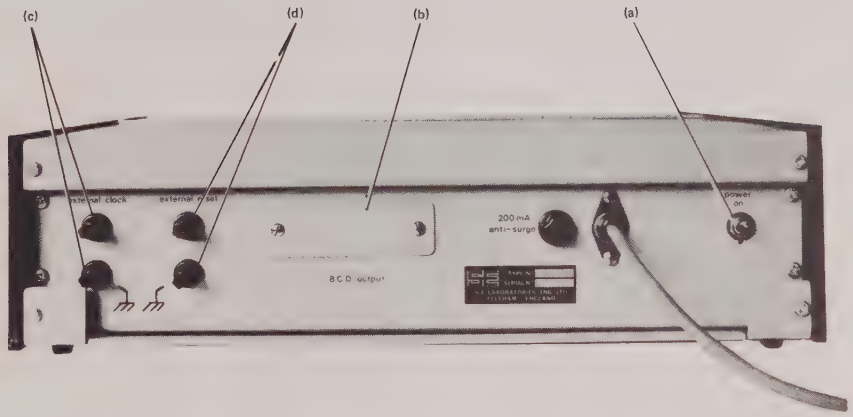
8.3.1. The period or pulsewidth of a signal applied to INPUT A is measured in terms of the internal clock oscillator. The frequency limit is 10Hz to 10MHz. With pulsewidth measurements, the minimum pulsewidth is 50ns. Maximum pulsewidth is 50ms. With period measurement there is no maximum limit.

(a) Connect the signal to be measured to INPUT A.

(b) Set the controls as follows:

(i) Select the PERIOD A push-button.

(ii) Set the PULSEWIDTH:PERIOD toggle switch to the type of measurement required (see fig 3.5.).



BASIC SM201 SHOWN

(a) POWER ON/OFF

(b) PRINTER OUTPUT SOCKET POSITION

(c) EXTERNAL CLOCK INPUT SOCKETS

(d) EXTERNAL RESET INPUT SOCKETS

FIG. 3.4. CONTROLS AND CONNECTORS – REAR PANEL

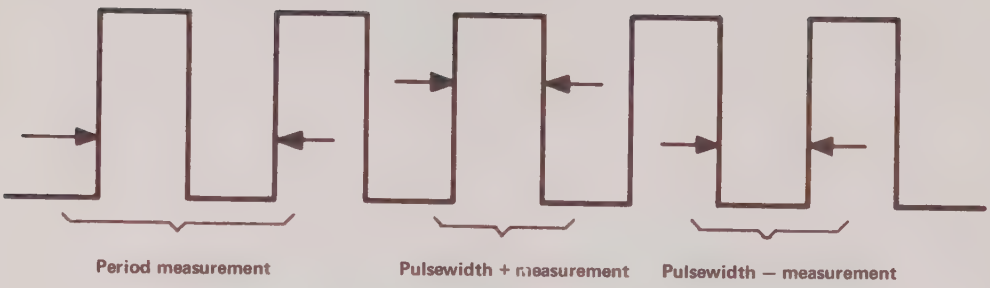


FIG. 3.5. PERIOD AND PULSEWIDTH MEASUREMENT

(c) Select the appropriate range:

(i) When only the frequency is approximately known (amplitude unknown) select the relevant range push-button and adjust the LEVEL and SENSITIVITY controls, if necessary (see ***Application Notes).***

(ii) When the frequency of the input signal is unknown, select range 1 and then 'range down' until the required resolution is obtained.

Range (left to right)	Time Units	Full Scale Reading (seconds)
1	1 µs	0.999999
2	10 µs	9.99999
3	100 µs	99.9999
4	1 ms	999.999
5	10 ms	9999.99
6	100 ms	99999.9

NOTE: Pulsewidth can be also measured by selecting the Time mode and using the Time and Count gating controls (see Para 8.6.2.).

8.4. Average Period Measurement

8.4.1. In this mode, the time over a number of periods is measured, the number being determined by the range selected. By the positioning of the decimal point, the display then gives the average time for one period in microseconds. Frequency and pulsewidth limits are as for period:

(a) Connect the signal to be measured to INPUT A.

(b) Depress the AVERAGE PERIOD push-button.

(c) Select the appropriate Range:

Range (left to right)	Number of Periods	Full Scale Reading (μs)
1	1	999999.
2	10	99999.9
3	100	9999.99
4	1000	999.999
5	10000	99.9999
6	100000	9.99999

(d) Adjust the LEVEL and SENSITIVITY controls if necessary (see ***Application Notes).***

8.5 Count Measurement

8.5.1. In this mode, the instrument counts signals applied to INPUT A. The frequency limits to which the instrument is capable of counting varies with the range selected (100MHz for range 1 and 10MHz for all other ranges). Frequency and pulsewidth limits are as for frequency mode on range 1 and as for period on other ranges. Set the controls as follows:

(a) Depress the COUNT A push-button and select the appropriate range.

NOTE: The count is divided by the number engraved above the selected range button (e.g. the 10^3 range push-button divides the count by 1000. To get ***true*** count, multiply by 10^2, 10^3, etc.)

(b) One of three methods can now be used to start and stop the count. These are described in Para 8.7, ***Time/Count Gating Controls.*** Adjust the LEVEL and SENSITIVITY controls , if required(see ***Application Notes***).

8.6 Time Measurement

8.6.1. In this mode, the instrument operates as an elapsed time meter with ranges selected in the same way as for the single period measurement (Para. 8.3):

(a) Depress the TIME SECS push-button and select the range. The ranges for this mode are as shown below:

Range (left to right)	Time Units	Full Scale Reading (in seconds)
1	1 μs	0.999999
2	10 μs	9.99999
3	100 μs	99.9999
4	1 ms	999.999
5	10 ms	9999.99
6	100 ms	99999.9

(b) One of three methods can now be used to shart and stop the timing sequence. These are described in Para. 8.7, ***Time/Count Gating Controls.***

8.6.2. ***Pulsewidth Measurement.*** The time mode can also be used to measure pulse width as follows:

(a) Connect the signal to be measured to the INPUT B and INPUT C connectors (linked together).

(b) Depress the B-C push-button.

(c) Set the POSITIVE: NEGATIVE: MANUAL toggle switches as follows:

(i) INPUT B to POSITIVE.
(ii) INPUT C to NEGATIVE.

(d) Depress the TIME SECS push-button and select the appropriate range. The pulsewidth is measured as shown in fig. 3.6. The positions of the toggle switches can be reversed to measure a negative - going pulse.

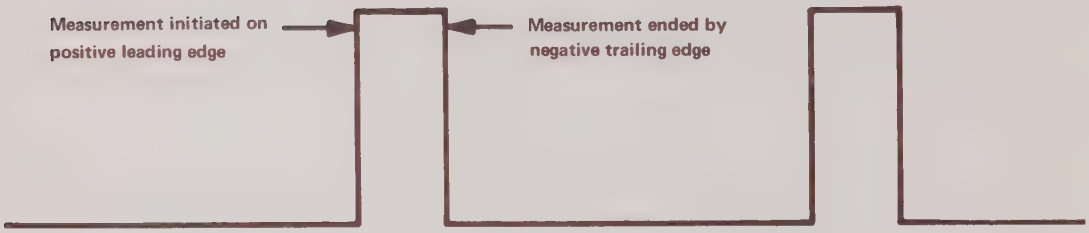


FIG. 3.6. TIME MODE – PULSEWIDTH MEASUREMENT

8.7 Time and Count Gating Controls.

8.7.1. The interval that is to be timed, or during which signals on INPUT A are to be counted, can be defined electrically or manually using the TIME/COUNT GATING controls and INPUTS B and C where appropriate. One of three methods can be employed:

(a) **Method 1: Manual Start:Stop.** In this mode, the INPUT B and INPUT C connectors are ***not*** used.

(i) Select B-B push-button.

(ii) Start count (or timing sequence) by pressing associated POSITIVE: NEGATIVE: MANUAL switch to MANUAL.

(iii) Stop count (or timing sequence) by pressing to MANUAL a second time.

—— OR ——

(i) Select B-C push-button

(ii) Start count (or timing sequence) by pressing (and releasing the POSITIVE:NEGATIVE:MANUAL switch to MANUAL (associated with INPUT B channel).

(iii) Stop count (or timing sequence) by pressing (and releasing) the POSITIVE: NEGATIVE: MANUAL switch to MANUAL (associated with the INPUT C channel).

(b) **Method 2: Signal Operated Start:Stop.** With this method, the count (or timing sequence) can be controlled by using one of the two gating modes:

(i) ***Gating Mode B-B:*** The count (or timing sequence) is started ***and*** stopped by a signal applied to the INPUT B connector provided the B-B push-button has been selected. The instrument counts the number of signals or time units on INPUT A between consecutive voltage transitions of the ***same*** polarity on INPUT B. The operative transition can be of either polarity and is selected by the POSITIVE: NEGATIVE: MANUAL switch associated with the INPUT B channel.

(ii) ***Gating Mode B-C.:*** The B-C push-button is selected. The count (or timing sequence) is started by a signal applied to the INPUT B connector and is stopped by a signal applied to the INPUT C connector. The instrument counts the number of signals or time units on INPUT A between a voltage transition on the INPUT B connector and one on the input C connector. The polarity of the operative transition can be selected by the POSITIVE: NEGATIVE: MANUAL switch associated with the INPUT B-C channel.

(c) **Method 3: Contact Closure Start:Stop**

(i) Closing the input high side of the INPUT B or INPUT C connector to chassis is equivalent to a logic 1 to logic 0 transition on the INPUT connectors.

(ii) Opening the input high side of the INPUT B or INPUT C connector is equivalent to a logic 0 to logic 1 transition on the INPUT connectors.

CAUTION

Mechanical relays and switches possess inherent contact bounce. To avoid any malfunction, therefore, select the B-C mode of gating using separate relays or switches for each channel (B and C), and arrange the contact closure timing so that each operation is followed by its return ***before*** the other channel operates.

8.8 External Clock Operation

8.8.1. When an externally derived clock oscillator is to be used to drive the instrument, the EXTERNAL CLOCK push-button on the front panel must be selected and the external clock input should be applied to the two input sockets provided on the rear panel. The frequency limit is 1kHz to 10MHz. In all other aspects, the instrument is then operated as with the internal clock operation. The maximum amplitude is 70V r.m.s.. The minimum rate of change is 40mV/μSec.

8.8.2. ***Calculation of Results*** When the externally applied clock oscillator frequency is other than 1 MHz, the displayed reading of a measurement will be wrongly scaled. The calculation required to obtain the true reading differs, depending upon the measurement mode in use:

(a) Period and Time Modes:

$$\text{True Reading (seconds)} = \text{Displayed Reading (seconds)} \times \frac{1\ \text{MHz}}{\text{External Clock Frequency}}$$

(b) Average Period Mode:

$$\text{True Reading } (\mu s) = \text{Displayed Reading } (\mu s) \times \frac{1 \text{ MHz}}{\text{External Clock Frequency.}}$$

(c) Frequency Mode:

$$\text{True Reading (kHz) (MHz)} = \text{Displayed Reading (kHz) (MHz)} \times \frac{\text{External Clock Frequency}}{1 \text{ MHz}}$$

8.9 Ratio Measurements.

8.9.1. ***Frequency Mode.*** The instrument is set-up as for the frequency mode using the external clock facility. The gate time is now controlled by the external oscillator frequency. Thus, if the external clock frequency is F_{ext} and the INPUT A frequency is Fi/p, the instrument reads:

$$\frac{Fi/p}{F_{ext}} \quad \text{on ranges 1, 2 and 3.}$$

$$\text{and} \quad \frac{Fi/p}{F_{ext}} \times 10^3 \text{ on ranges 4, 5 and 6.}$$

NOTE: Both frequencies must be expressed in the same units .

8.9.2. ***Period Mode.*** The period of the INPUT A signal is measured in terms of the external clock oscillator period. The instrument reads (on all ranges):

$$\frac{F_{ext}}{Fi/p} \times 10^{-6}$$

NOTE: Both frequencies must be expressed in the same units.

8.9.3. ***Average Period Mode.*** The instrument measures the average period of the signal applied to the INPUT A connector in terms of the external clock oscillator period. The instrument reads (on all ranges):

$$\frac{F_{ext}}{Fi/p}$$

NOTE: Both frequencies must be expressed in the same units.

8.10 Hold and Reset Facility

8.10.1. To hold a reading in any mode, depress the HOLD push-button. A new reading can be obtained either by:

(a) pressing the RESET push-button (when the reading is reset to zero) then releasing it (when a new measurement

sequence may start and this reading will be held) or,

(b) application of a reset signal to the external reset input connector on the rear panel; logic 0 (0 V to + 0.4 V) activates reset, logic 1 (+ 2.4 V to + 5 V) initiates a new measurement sequence.

9. APPLICATION NOTES

9.1 Effects of Noise on Frequency and Count Measurements

9.1.1. Excessive noise superimposed on the input signal can result in erroneous readings. The LEVEL and SENSITIVITY controls should be adjusted in conjunction to obtain the best results. The effect of noise on the accuracy of the internal counting circuits is illustrated in fig. 3.7B.

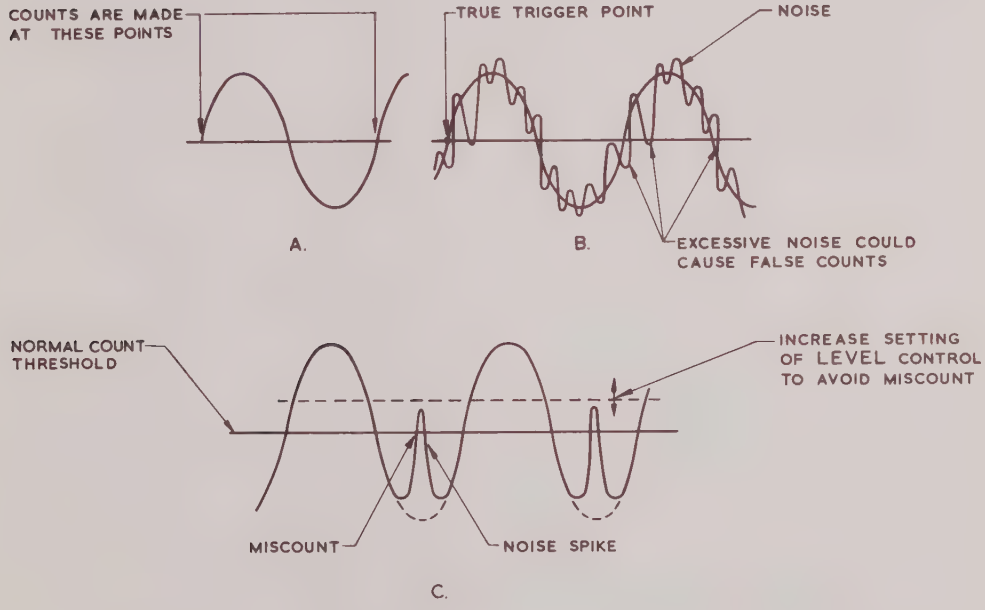


FIG. 3.7. NOISE ON FREQUENCY AND COUNT MEASUREMENTS

9.1.2. With a signal similar to that in fig. 3.7.B the SENSITIVITY switch should be used to attenuate the overall signal and the LEVEL control adjusted so that the counter circuit is triggered at the correct points.

9.1.3. Miscounts can also be caused by the type of superimposed noise illustrated in fig. 3.7.C. To avoid this, increase the setting of the LEVEL control. If the counting circuit is still miscounting, adjust the setting of the SENSITIVITY switch and re-adjust the level control.

9.2 Effects of Noise on Single Period Measurements.

9.2.1. Where a small amount of external noise is present on the signal, an effect can occur where the noise triggers the counting

circuit just prior to the true signal trigger point, as shown in fig. 3.8.

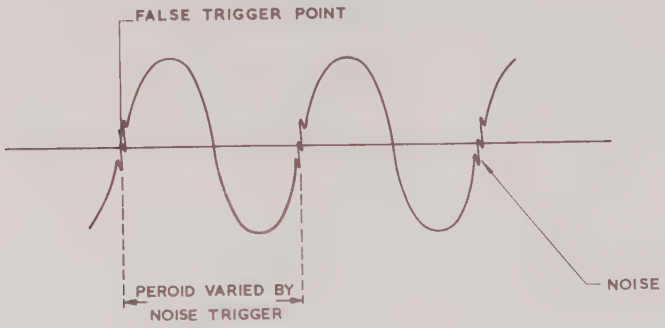


FIG. 3.8. NOISE ON SINGLE PERIOD MEASUREMENTS.

This results in each period varying from the next in length, giving an overall 'jitter' effect to the displayed reading. This can be reduced by using the AVERAGE PERIOD mode.

9.3 Pulsewidth Measurement

9.3.1. Inaccuracies in readings can occur where a sawtooth or ramp type pulse is being measured due to the effect shown in fig. 3.9.

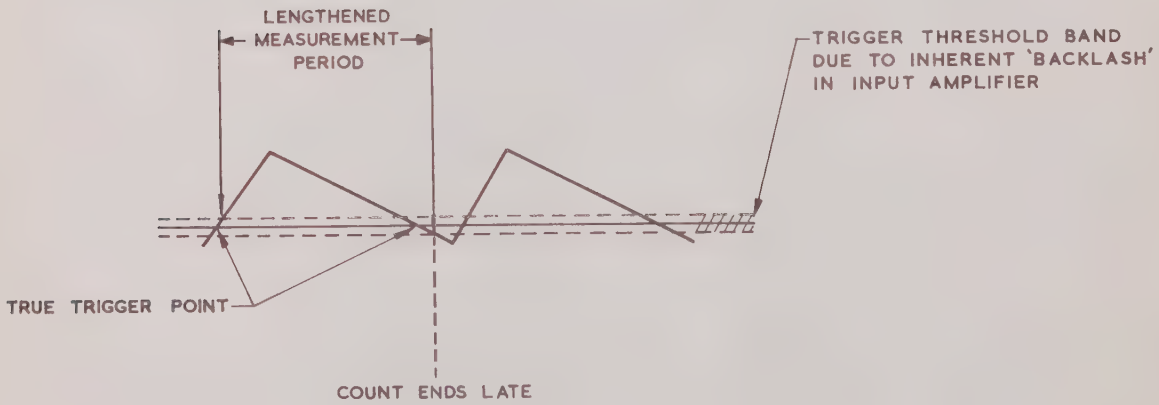


FIG. 3.9. ERRORS ENCOUNTERED WITH RAMP INPUT WAVEFORMS

9.3.2. This effect occurs only when a marked difference exists between the rise and fall times of a waveform such as found with a ramp. From fig. 3.9 it can be seen that the instrument is measuring a longer period than actually exists. A longer delay before counting stops is caused by the more gradual slope of the trailing edge than was experienced with the leading edge to start the count. This can be minimised by setting the SENSITIVITY switch to the most sensitive setting to make the input signal as large as possible . The LEVEL control should be ideally set to the mean of the pulse.

SECTION 4

TECHNICAL DESCRIPTION

1. INTRODUCTION

1.1 Timer/Counter SM201, for purposes of circuit description, can be considered as seven major sub-assemblies:

(a) Input Amplifier Board. This contains the signal input (input A) amplifier and the first decade (units) of the counting circuit. The first stage of the second counting decade is also mounted on this board.

(b) Display and Logic Board. This contains the remaining decades of the counting circuit and the associated display store logic, decoding logic and numerical indicator tubes. Also mounted on this board are the control logic, internal clock oscillator, external clock input amplifier and the inputs B and C gating logic.

(c) Switch Board Assembly. This provides the interconnections between the push-button switches and the Display and Logic Board.

(d) Front Panel Assembly. All operator controls except the POWER ON switch and push-buttons are mounted on this assembly.

(e) Rear Panel Assembly. On this is mounted the printer connector, external reset and clock sockets, mains fuse and POWER ON switch.

(f) BCD Outputs Unit SM244. This comprises a p.c. board and a 34-way connector. The p.c. board carries a number of integrated circuit buffers for the BCD outputs, and logic gates for the overrange and print command functions.

(g) Power Supply Unit. This consists of the mains transformer and a stabiliser p.c. board.

A block schematic is shown in fig. 4.1. below

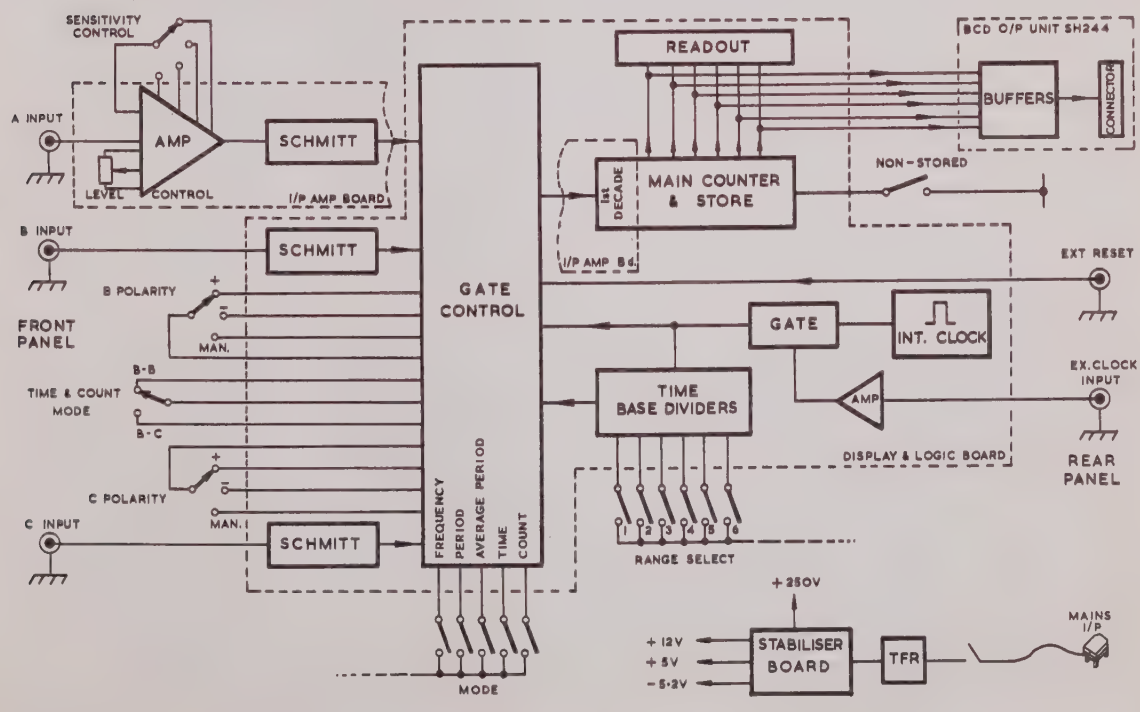


FIG 4.1 TIMER/COUNTER SM 201– BLOCK SCHEMATIC

2. INPUT AMPLIFIER

2.1 The input amplifier can be divided into 3 basic circuits as follows:

(a) input R-C attenuator with frequency compensation.

(b) a.c. amplifier and Schmitt trigger

(c) d.c. feedback loop

2.2 **The input attenuator** is formed by resistors R1s to R7s and capacitors C1s to C5s; the resistors provide attenuation at low frequencies and the capacitors at high frequencies. The input signal is a.c. coupled by capacitor C4s.

2.3 **A.C. Amplifier.** The a.c. signal is fed via the input attenuator and the limiter (D1, D2, R1, C14) to the gate of source-follower TR1; the source follower is incorporated to provide a high input impedance. The source output of TR1 is applied to the base of TR2, which forms part of the long-tailed pair stage TR2, TR4 with constant current provided by TR3 in the tail. The gain of the long-tailed pair is defined by resistors R10 and R11. The output of this stage is taken from the collectors via TR6 and TR7 to the Schmitt Trigger Stage TR8 and TR9. As the collectors of TR8 and TR9 are connected (via R33 and R35) to the 0V line and the emitters to the −5.2V line (via R36) the squarewave output (at the frequency of the output A signal) is between −0.7V and −2.0V (nominal values), these being the levels required for the counting logic mounted on the input amplifier board.

2.4 **The d.c. feedback loop** is required to compensate for temperature drift in the source follower stages TR1 and TR5. D.C. feedback is provided by the transistor pair IC10 which senses the signal output level applied at TR6 collector. This a.c. component is smoothed by capacitor C7, so that a d.c. level is applied to IC10, pin 4 (base). The output at IC10, pin 1 (collector) is applied via source-follower TR5 to TR4 base.

2.5 An offset current is also applied to IC10, pin 4 by the LEVEL control which has the effect of moving the d.c. base line about which the a.c. component alternates at TR6 collector.

2.6 Ferrite beads X1 and X2 are included in the +12V and −5.2V supply lines as decoupling inductors to reduce effects by high-frequency noise.

3 DISPLAY AND LOGIC BOARD

3.1 The description of the logic on this board is given in terms of the modes of operation, with the control logic considered separately.

3.2 **Frequency Mode (Fig 1A)**

3.2.1 In the frequency mode, the signal-to-be-measured is sampled for a set period of time, determined by the divider output selected by the range push-buttons.

3.2.2 The signal-to-be-measured is routed via the input amplifier circuit to the J-K (pins 5 and 10) input of bistable IC6/13 on the input amplifier board. It must be noted that this bistable is the first stage of the first decade of the counter, the remaining stages being IC1, IC2 and IC3. The output of bistable IC6/13 is fed into latching bistable IC5, the output of which is applied to gate IC8/3.

3.2.3 Gate IC8/3 is enabled in the frequency mode, by depressing the FREQ push-button; the action is as follows. With FREQ depressed, a logic O is applied to gate IC4/11 which, in turn, applies a logic 1 (routed via resistors R2, R3) to

the 'channel select' gates IC9/8 and IC9/6. The logic O output of gate IC9/8 enables gates IC8/3 and IC8/8 so that the incoming signal can be applied to the remainder of the 1st counter to produce 1, 2, 4, 8, outputs at pins 1, 2, 3 and 4 respectively on the input amplifier board.

3.2.4 The length of time that the incoming signal is allowed to drive the counter is determined by the 'stop 1' and 'stop 2' inputs to the latching bistables IC5/12 and IC5/2 on the input amplifier board,(these are at logic 1 to enable). These are controlled by the output of the 'stop' bistable IC18/12, which in turn is governed by the selected divider output, selected by the range switches.

3.2.5 The divider is fed with the 1 MHz output pulse train of the clock oscillator, via gates IC15/6, 15/11, 14/8 to the first ÷ 10 divider element IC23. The divider chain comprises IC23 to 29 inclusive and the 1, 10, 10^2, 10^3, 10^4 and 10^5 outputs are applied to the range selection gates (IC's 10/10, 10/3, 10/4, 10/2, 11/8 and 11/13). Each gate is connected to a range push-button, which when depressed enables the gate. The output of the range selection gates is routed via gates IC10/8 and 3/3 to the 'gate open' bistable IC19/8. The logic operation from this point is similar for all modes of operation and is described in **Para. 3.7 Control Logic Sequence of Operation.**

3.3 **Period and Pulsewidth Modes (fig. 1B)**

3.3.1 In the period mode, the instrument measures the period of the signal-to-be-measured in terms of the internal clock oscillator. With the front panel toggle switch SW3a and 3b set to positive or negative pulsewidth position (and with the PERIOD push-button depressed), the corresponding pulsewidth of the signal is measured in terms of the internal clock oscillator.

3.3.2 The incoming signal is used to control the gate open and channel select logic, and the divider output is applied to the counting circuits.

3.3.4 The signal path is as follows. The signal is routed via R40 and gate IC9/3 on the input amplifier board and via TR17 on the main logic board to gate IC4/6. Here, the signal is inverted and both polarities are applied to the polarity selection gates on IC16.

3.3.5 On period measurements, the incoming signal applied to gate IC16/3 is enabled by input pin 2 of the gate being open-circuit by operation of the PERIOD A SECS push-button.

3.3.6 On pulsewidth measurements, the input signal and its inverse are applied to gates IC16/3 and IC16/1 respectively. Depending upon what polarity is selected by SW3a and b, so depends which gate is enabled.

SW3 Position	Gate Enabled	Gate Inhibited
+	IC16/1	IC16/3
—	IC16/3	IC16/1
Period	IC16/3	IC16/1

3.3.7 The signal is then applied to the multi-input NOR gate IC16/8, the output of which is applied as the clock input to the 'gate open' bistable IC18/8. It is also applied to gate IC9/11 which is enabled only on pulsewidth measurement (pin 13 is open-circuit, unless SW3 is on PERIOD). The logic operation from this point is similar for all modes of operation and is described in **Para. 3.7 Control Logic Sequence of Operation.**

3.3.8 The clock oscillator output is applied to the third decade of the divider via gates IC15/11, IC14/6 and IC6/8 and the 1, 10, 10^2, 10^3, 10^4, 10^5 outputs are applied to the range selection gates (IC's10/10, 10/1, 10/5, 10/2, 11/8 and 11/13). The selected output is fed via gate IC10/8, IC3/6, IC3/11, and the level changing network R10, R11 to the input amplifier board. Here, it is applied to the J/K input (pin 6 and 9) of bistable IC7/13, which now forms the first stage of the first decade of the counter. Thus, the length of time that the counter is allowed to count is controlled by the period or pulse-width duration of the incoming signal.

3.4 Average Period Mode (fig 1C)

3.4.1 In this mode, the instrument measures the average period of a signal applied to the A INPUT. The display indicates an average period measured over a series of periods up to 10^5 as determined by the range selectors.

3.4.2 The signal-to-be-measured is fed via gate IC9/3 on the input amplifier board to TR17 on the main logic board. After level changing has occured at this point, the signal is routed via gates IC4/8, 6/8 to the divider decades IC25 to IC29. The selected output is applied to the clock input of 'gates open' bistable IC19/8. From this point, the logic operation for the 'gate open & close' sequence is similar for all modes and is described in **Para 3.7 Control Logic Sequence of Operation.**

3.4.3 From this, it can be seen that the incoming signal is controlling the duration of the count. The counter is driven by the clock oscillator pulse train, which is routed via gates 15/6, 15/11, 14/3, 8/8, 3/13 and the level changing network R10, R11, R12 and D4, to bistable IC7/13 on the input amplifier board.

3.4.4 The 'Stop 2' input to latch IC5/2 is at logic 1 at this time, so that the output of bistable IC7/13 is passed through to gates 8/13 and 8/6. These gates are enabled by a logic O level fed from gate IC9/6, this being determined by the fact that pin 'm' (the input to gate 4/11 on the main logic board) is open-circuit (floating), at this time.

3.5 Time Mode (fig 1D)

3.5.1 In this mode, the instrument operates as an elapsed time meter.

3.5.2 The internal clock oscillator pulse train is applied to the divider chain at pin 14 of IC25, via the gate path IC15/6, 15/11, 14/6, and 6/8. The outputs of the divider (1, 10, 10^2, 10^3, 10^4, 10^5) are applied to the range selection gates, and the selected output is fed via gates IC10/8, 3/6 and 3/11 and the level changing network R10, R12 and D4 to bistable IC7/13 on the input amplifier board. This is the first stage of the first counter decade and the output is applied to the S input of the latch bistable IC5/2. In this mode, the stop 2 input is at logic 1 and the counter input is fed through to the channel select gates of which IC8/6 and 8/11 are enabled. The counter continues counting until the 'stop' bistable IC18/13 (on the main logic board) sets a logic O into the CP (stop 2) input of bistable IC 5/2.

3.5.3 If a signal is connected to INPUT A during a time measurement it will not interfere with the logic operation as gates IC4/8 and IC16/13, 16/2 on the main logic board, are inhibited and the 'stop 1' input to bistable IC5/12 on the input amplifier board is held at logic O.

3.5.4 The duration of the count is controlled by the gating logic in the same way as for the count mode. See Para. 3.6.4.

3.6 Count Mode (fig 1E)

3.6.1 The count mode logic operation differs depending upon whether Range 1 is selected or not. The signal-to-be-measured is applied to the counting circuit, and the length of time that the counter is allowed to count is determined by the gate open (start) and close (stop) signal derived from the start/stop inputs (B and C).

3.6.2 ***Range 1 Operation.*** On range 1, the incoming signal-to-be-counted is applied directly from the input amplifier to the first bistable, IC6/13, of the first decade of the counter. On range 1, the depressed range 1 push-button connects input pin 12 of gate IC4/11 to OV (with COUNT A also depressed) so that the channel select gate IC9/8 enables gates IC8/3 and IC8/8. Thus the 1st decade of the counter starts counting. On all other ranges of the COUNT mode, the channel select gate inhibits gates IC8/3 and IC8/8.

3.6.3 ***Range 2, 3, 4, 5 and 6 Operation.*** On these ranges, the incoming signal-to-be-counted is fed via gate IC9/3 on the input amplifier board to TR17 on the main logic board. From here, it is fed via gates IC4/8 and IC6/9 to the divider logic.

The 10, 10^2, 10^3, 10^4 and 10^5 outputs from the divider are applied to the range selection gates and depending upon the range selected,one output is fed via gates IC3/6, IC3/11, and level changing network R10, R11 to IC7/13 on the input amplifier board.

3.6.4 ***Gating Logic, B-B Gating Operation.*** The B-B push-button is mechanically coupled to the B-C push-button, so that when the B-B push-button is depressed, it releases the B-C push-button. In this state, the j input pin of bistable IC22/13 is linked via the B-C switch to OV and the k input of bistable 22/9 is open circuit. This means that bistable 22/13 is inhibited so that any spurious signals appearing on the 'c' line will not affect the B-B operation. One of two methods of generating a start/stop (gate open/gate closed) signal can be used:

(a) Manual Gating on Input B. When the B POSITIVE: NEGATIVE: MANUAL: toggle switch SW2 is depressed to manual, input pin 12 of gate 12/11 is taken to OV (pin 1 of gate IC47 at this instant being open-circuit and therefore enabling the gate) so that a negative going transition is generated at NOR gate 47/8. (**NOTE:** IC47/8 and gate 12/8 form a latch to prevent contact bounce effects when SW2 is pressed). The transition on gate 47/8 clocks bistable 22/9, via SW3b, to produce a logic O output at QIC22. This output is twice inverted by gates 16/5 and 16/8 and applied as the clock input to 'gate-open' bistable 18/8.

(b) Signal Gating on Input B. When a signal on INPUT B is used to initiate the gating sequence, it is applied to the base of transistor TR9 causing it to switch between OV and +5V (approx). This ensures that the incoming signal is always reduced to between switching levels of OV and +5V. For positive transient gating, (on input B) the output of TR9 is coupled directly as a negative-going transient to the clock input of bistable IC22/9, via SW2b. For each negative transient (on input B) the output of TR9 is fed via inverting gates IC47/9 and IC47/8 and applied via SW2b as a negative going transient to the clock input of bistable IC22/9.

3.6.5 ***Gating Logic, B-C Operation.*** When the B-C push-button is depressed, the J input of bistable 22/13 is disconnected from the OV line (open-circuit) and the k input to bistable 22/9 is connected to OV. When a start pulse appears on the B line, Q22/9 goes to logic 1 and stays on 1 even if other pulses are subsequently applied. When a stop pulse appears on the C line, $\overline{Q}$22/13 changes to logic O, resetting bistable 22/9 via gates 17/3 and 17/11. These gates also form an AND gate so that the manual RESET push-button can also reset bistable 22/9.

3.6.6 The manual (stop) gating on the input C line follows the same principle as on input B.

3.7 Control Logic-Sequence of Operation (fig 1F)

3.7.1 The following paragraphs outline the sequence of operation with stored display selected and the HOLD and RESET push-buttons not selected. Non-stored display operation and manual HOLD and RESET operation are discussed under separate headings.

3.7.2 As previously mentioned under the mode descriptions, the gate open signal is applied to either bistable 19/8 (Frequency and Average Period Modes) or 18/8 (Time, Count, Period and Pulse width Modes). Both outputs affect the output of gate 7/6, which in turn, affects the remainder of the control logic during the 'gate-open' period. The state of the control logic outputs is as follows (see also fig 4.2 Timing Diagram for Control Logic):

(a) gate 7/6 is at logic O,
(b) gate 8/3 is at logic 1,
(c) 'stop' bistable Q18/12 at logic O,
(d) 'reset' bistable Q21/12 at logic O,
(e) 'transfer' bistable Q19/12 at logic O,
(f) gate 8/6 at logic 1,

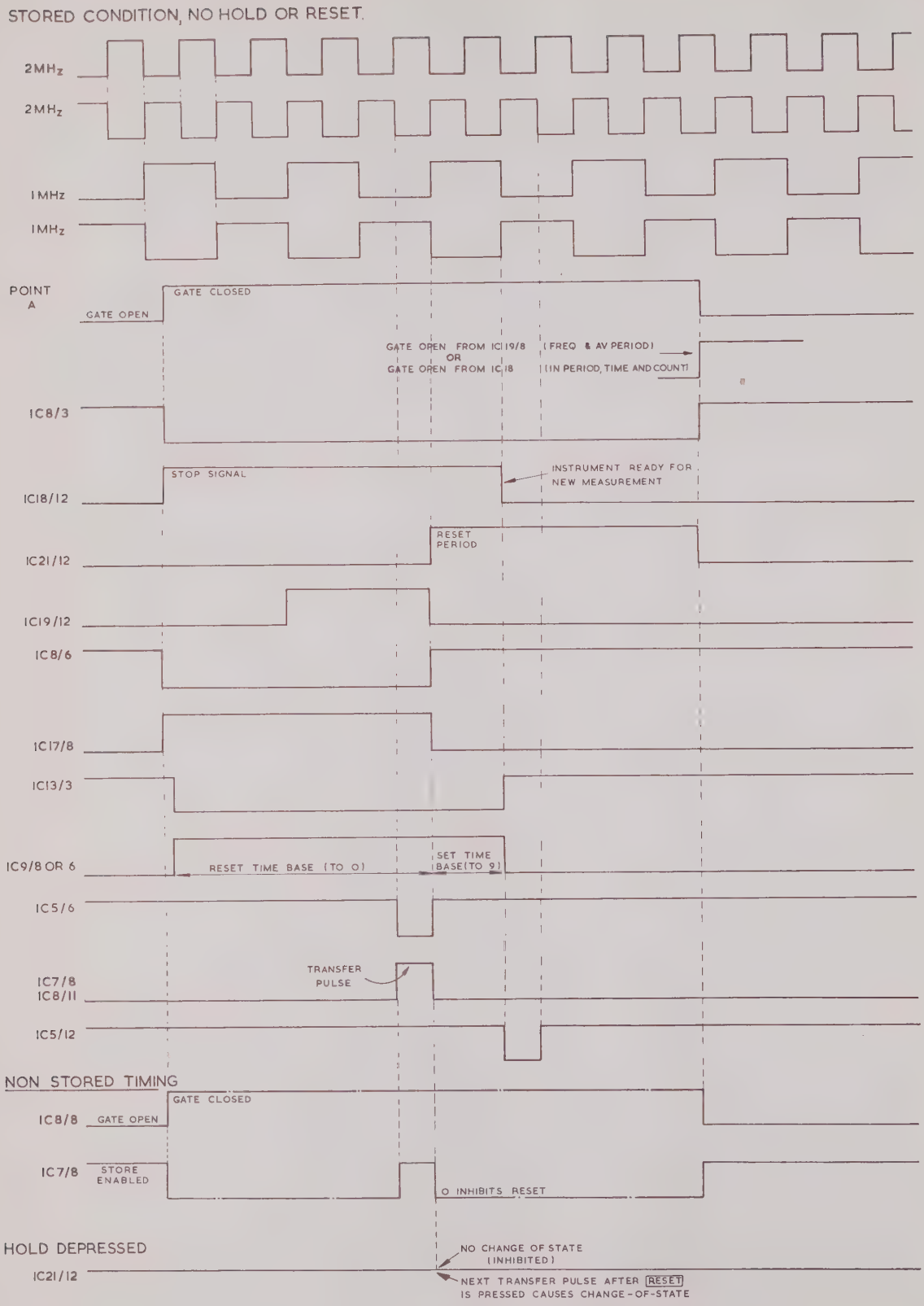


FIG 4.2 TIMING DIAGRAM FOR CONTROL LOGIC

(g) gate 17/8 at logic O,
(h) gate 13/3 at logic 1,
(j) gates 9/8 and 9/6 at logic O,
(k) gate 5/6 at logic 1,
(m) gates 7/8 and 8/11 at logic O
(n) gate 5/12 at logic 1

3.7.3 With gate 7/6 at logic O, transistor TR14 is cut off and the GATE OPEN indicator lights-up. At the end of the 'gate-open' period, the output of gate 7/6 changes to logic 1, the GATE OPEN indicator is extinguished, and the state of the control logic output points changes as follows:

(a) output of gate 8/3 drops to logic O,
(b) Q output of 'stop' bistable 18/12 changes to logic 1,
(c) output of gate 8/6 changes to logic O,
(d) output of gate 17/8 changes to logic 1,
(e) output of gate 13/3 drops to logic O,
(f) output of gates 9/8 and 9/6 changes to logic 1.

Gates 9/8 and 9/6 at logic 1, reset the divider decades to zero.

3.7.4 At this point the control logic employs the 2MHz, $\overline{2MHz}$, 1MHz and $\overline{1MHz}$ outputs of the internal clock oscillator to continue the sequence. With the logic in the state listed above, the next negative-going transient of the $\overline{1MHz}$ output of bistable 20/8 clocks 'transfer' bistable 19/12, setting its Q output to logic 1. This is applied to gate 5/6 which also gates together the 2MHz output from TR18 (on pin 3) and the $\overline{1MHz}$ $\overline{Q}$ output of bistable 20/8. This causes the output of gate 5/6 to drop to logic O, returning to logic 1 at the next $\overline{1MHz}$ negative-going transient at pin 4. The inverse of this pulse appears at the output of gates 7/8 and 8/11, this being the transfer pulse. This is fed to the stores on the main counter circuit as the 'store gate pulse' transferring the counter value reached during the gate-open period to the counter store, and thus to the indicator tubes.

3.7.5 The negative-going trailing edge of the transfer pulse, at the output of gate 8/11, clocks the 'reset' bistable 21/12, causing $\overline{Q}$21/12 to change to logic O. This is the start of the 'reset' period, and causes the outputs of gates 8/6 and 17/8 to change state to logic 1 and logic O respectively. This level change sets the divider decades to 9.

3.7.6 Q21/12 applies a logic 1 to gate 5/12 which also gates in the $\overline{2MHz}$ clock and the $\overline{1MHz}$ clock pulse trains. When all input pins are at logic 1, the output of gate 5/12 drops to logic O and this level is applied to the 'clear' input pin (2) of the 'stop' bistable 18/12. This causes $\overline{Q}$18/12 to change to logic O removing the stop signal from the channel select gates, thus enabling the counter for the next measurement sequence. The output of gate 13/3 changes to logic 1 causing the outputs of gates 9/6 and 9/8 to change to logic O ready for the next gate open period. Setting the divider decades to O earlier on in the sequence and then setting it to 9 at this time, enables the instrument to be immediately ready for the next measurement sequence.

3.7.7 ***NON-STORED Display Selected (fig 4.2)*** With the NON-STORED push-button depressed, a logic 1 is applied to pin 10 of gate 8/8. Pin 9 of this gate is also at logic 1 during the gate open period. A logic O is therefore applied to pin 12 of gate 7/8, the output of which is at logic 1 during the gate open period, thus enabling the store. The counter value is therefore shown by the numerical indicator tubes as the count value builds up. At the end of the measurement, the gate closed period starts and the output of gate 8/8 changes to logic 1. The output of gate 7/8 goes to logic O, inhibiting t store thus holding the reading, until the start of the next measurement.

3.7.8 ***Manual HOLD and RESET Selected (fig 4.2)*** With the HOLD push-button selected, pin 9 of gate 5/8 is at logic 1, so that

the J input of bistable 21/12 is at logic O and the bistable is inhibited. This means that when the transfer pulse occurs, its trailing edge has no effect on this bistable (see Para. 3.7.4.) and no reset period occurs. Gate 5/6 continues generating transfer pulses as subsequent measuring sequences occur, but these also have no effect. However, when the RESET push-button is depressed, (or an external reset signal is applied) the J pin of bistable 21/12 changes to logic 1 and the instrument is reset on the occurrence of the next transfer pulse.

3.8 COUNTER CIRCUIT

3.8.1 The counter circuit is distributed over two p.c. boards as follows:

(a) ***Input Amplifier Board*** This contains the first (units) decade (1248) and the first stage (10) of the second decade.

(b) ***Display and Logic Board*** This board contains:

(i) level changing stages, connecting the (a) above components to the remaining decades on the display and logic board.

(ii) last three stages of the second decade and the remaing counter decades, six stores, six decoders and six numerical indicator tubes.

(iii) overrange bistable, fed from the sixth decade on the display and logic board.

3.8.2 On the input amplifier board, the first decade of the counter is split between the first bistable (1) and the remaining three bistables (2, 4 and 8). This first bistable is selected from one of two bistables, IC7 or IC6, depending upon which operating mode has been selected. This is shown in the table below:

Mode	Bistable Selected	Triggered By
Frequency	IC6	Incoming signal
Period/Pulsewidth	IC7	Internal Clock
Count (Range 2–6)	IC7	Internal Clock
Count (Range 1)	IC6	Incoming signal
Time	IC7	Internal Clock
Average Period	IC7	Internal Clock

3.8.3 Each bistable is connected to the remaining stages of the 1st decade by a latch and two channel selecting gates. A logic 1 applied to the clock input of each latch enables it and the output of the first selected bistable is passed through to the channel select gates on IC8. These are controlled by the channel select input applied to gate 9/8; a logic O applied to a gate on IC8 enables it.

3.9 BCD OUTPUTS UNIT SM 244

3.9.1 This unit, which is fitted to the '/B' versions of the SM201 only, is an optional fitting for the basic version and can also be supplied in kit form. It consists of a p.c. board wired to a 34-way socket. The board is plugged into an edge connector on the display and logic board.

3.9.2 The board contains a total of forty-eight invertors, six to a package on ICs 2 to 9, which handle the BCD outputs. The over-range signal output is inverted by gate 1/11.

3.9.3 The BCD outputs should be used only when the counter is not counting (during the display time). The print command signal is provided so that the BCD outputs can be inhibited during the period when the counter is counting. This signal

is derived from the transfer pulse.

3.9.4 The transfer pulse is applied to gates 1/3, 1/6 and 1/8. Gates 1/6 and 1/8 are connected as a monostable, required to lengthen the transfer pulse to be greater than 15μs. This, then, becomes the printer command signal, the increased duration being required to drive an external printer.

3.9.5 The +5V d.c. input to the BCD board is protected on the board by a 250 mA fuse FS1, and is also further stablised by zener diode D1.

3.10 POWER SUPPLY

3.10.1 The power (mains) is fed via the mains input socket, switch SW5 and 200 mA fuse FS1 to the primary of mains transformer T1, the tappings of which are linked in series for 230V mains operation, or in parallel for 115V mains operation.

3.10.2 Five supplies are generated:

(a) +250V unstabllised d.c. supply for the numerical indicator tubes.

(b) +12V stabilised d.c. supply for the input amplifier board and clock oscillator, on the main logic board.

(c) +5V stabilised d.c. supply used for the integrated circuits, external clock input amplifier, clock oscillator (SM 201 only), external reset input circuit, external gating input circuits, all on the display and logic board and BCD board.

(d) -5.2V stabilised d.c. supply for the integrated circuits on the input amplifier board, the level inverting transistors and networks on the display and logic board.

(e) 8.5V–O–8.5V (approx.) a.c. supply for the high-stability clock oscillator, used on SM 201 H only.

3.10.3 ***+250V d.c. Supply.*** The +250V supply is derived from the half-wave rectifier D1 and the output is fed from wiring pin 6 of the power supply board.

3.10.4 ***+12V Supply.*** The +12V supply is half-wave rectified by diode D2 and stabilised by the differential amplifier IC1/1 controlling the base of series transistor TR1. The supply is then decoupled by capacitor C3.

3.10.5 ***+5V Supply.*** The +5V supply is full-wave rectified by diodes D3 and D4 and stabilised by amplifier IC1/8 controlling the bases of the series pair TR2, TR5.

3.10.6 ***–5.2V Supply.*** The –5.2V supply is full-wave rectified by diodes D5 and D6. The supply is stabilised by the differential amplifier IC1/14 controlling transistor TR 3. The potential on the base of series transistor TR 4 is controlled by TR 3 collector. The supply is set-up by adjusting RV 1.

SECTION 5

CALIBRATION

TEST EQUIPMENT REQUIRED

(a) Avometer Type 8. This should be calibrated at the following points:

5V (indicated) on the 10V D.C. range.
12V (indicated) on the 25V D.C. range.

The accuracy of the calibration system should be ± 0.1% of the voltage applied, or better.

(b) Jacel Frequency Meter Type 331 or Similar. The crystal oscillator and associated oven are to be run continuously to maintain optimum stability. Under these conditions, the instrument should be checked against the B.B.C. 200 kHz transmission every 14 days, by using an "Off Air" Standard.

The Frequency Meter and Off Air Standard outputs are to be compared for 300 seconds at least. This is to average out short term phase shifts in the Off Air Standard output. Also the comparison should take place over an integral number of cycles of drift to eliminate possible errors due to "pulling" between the two signals.

The difference should be recorded and allowed for when using the Frequency Meter.

(c) S.E. Laboratories Oscilloscope Type SM.112 with SM.599 Vertical Amplifier or Similar. This instrument should be calibrated on the 10 mV/cm range, the deflection being recorded for the following input signals:

80 MHz, 25 mV peak to peak
100 MHz, 45 mV peak to peak
110 MHz, 60 mV peak to peak

These signals should be set up using an oscilloscope with Tektronix type 1S1 sampling plug in unit, or similar 1GHz System.

(d) Signal Generator GR Type 1363 or Similar. Used with GR Power Supply Type 1267.

(e) Airmec Video Oscillator Type 339 or Similar.

(f) Levell Decade Oscillator Type TG.66A or Similar.

(g) Levell R.C. Oscillator Type TG.150D or Similar.

(h) Megger Insulation Tester (500V) or Similar.

(i) D.C. Voltage Source, 0 to 1.2V Range. This voltage is to be produced by resistive division of a supply of 5V d.c. or greater, to give an output impedance not greater than 75 ohms. Stability is not important, voltage levels as required by performance test specification are to be set up using Avometer, Item 1.0.(a)

Ripple to be less than 10 mV peak to peak.

The output may be produced by varying the resistor across which is developed. In this case the output is to be

decoupled by a 50 µF electrolytic capacitor. When used with an oscillator to provide a mixed d.c. and a.c. signal. the d.c. source is to be connected in series with the "Low" side of the oscillator.

2. PERFORMANCE CHECKS

(a) Connect instrument to supply and switch on.

Supply Checks

(b) Set -5.2V rail, using Avometer, Item 1.0. (a). Check that:

(i) +5V rail reads between +5.2V (max) +4.8V (min)

(ii) +12V rail reads between +12.7V (max) +12.1V (min)

(iii) Numerator tube supply (at 230V input) mean d.c. reads between +98V (max) +88V (min)

Decimal Point Checks

(c) Check decimal point operation (ranges numbered 1 to 6, left to right, also tubes numbered 1 to 6 left to right):

(i) Select COUNT mode ranges 1 to 6 in turn, should give no decimal points.

(ii) Select FREQUENCY mode, selecting ranges 1 to 6 in turn. This should give decimal points in tubes as follows:

Range	1	2	3	4	5	6
Tube	5	4	3	5	4	3

(iii) Select PERIOD mode. Check that decimal points appear as follows:

Range	1	2	3	4	5	6
Tube	1	2	3	4	5	6

(iv) Select AVERAGE PERIOD mode. Check that decimal points appear as follows:

Range	1	2	3	4	5	6
Tube	None	6	5	4	3	2

(v) Select TIME mode. Check that decimal points appear as follows:

Range	1	2	3	4	5	6
Tube	1	2	3	4	5	6

(d) **B-B, B-C (manual operation), Hold, Reset**

(i) Select TIME mode, 'B-B', operate RESET once. Check that successive operations of B toggle switch to MANUAL open and close the counter gate, as indicated by the GATE OPEN Lamp. Check that C channel is inoperative.

(ii) Check that with gate open, operating RESET once will close it.

(iii) Select HOLD, with gate closed. Check that operating B MANUAL opens and closes the gate once, and that further operations of B MANUAL do not operate the counter.

(iv) Clear HOLD, open the gate by using B MANUAL, select HOLD. Check that operating B MANUAL closes the gate, and that further operations of B MANUAL do not open it.

(v) Operate RESET once. Check one further cycle only of opening and closing the gate may be obtained.

(vi) Clear HOLD. Select B-C. Check that gate may be opened by B MANUAL, closed by C MANUAL. Check that with gate open B has no effect. Check that with gate closed, C has no effect.

(e) **Main Counter, Display, Range Selection.**

(i) Select TIME mode B-B,NON-STORED. Operate counter on each range in turn, from 6 to 1. Check that, while the gate is open, display is counting correctly. This check should be performed on each decade in turn, selecting the most convenient range (the slowest rate on tube 6 will be 1/10 second count, if this is too fast for convenient viewing, an external oscillator will have to be used as in step (k). Check that as the range is changed, the counting rate changes appropriately (this is an approximate check only).

(ii) Using range 2, note that as tube 1 display changes from 9 to 0 for the first time after the gate has been opened, the OVER RANGE lamp comes on and stays on as tube 1 changes from 9 to 0 a second and subsequent times.

(iii) Check that for each tube, using range most convenient, the display holds at the count attained when the gate is closed, and returns to 0 when the gate is re-opened.

(iv) Check that when NON-STORED is re-selected, display up-dates and continues to follow count.

(v) Check that with NON-STORED selected or cleared, gate open or closed, operating RESET once clears display to zero.

(f) **Frequency Mode**

(i) With the Avometer, check voltage limits at TR6 collector (input amplifier) as LEVEL control is varied. These should be from -1V +0.2V (anticlockwise) to -3V +0.2V (clockwise)

(ii) With the Avometer, check high and low states of trigger output at TR10 emitter (input amplifier). Operate 'Level' control to trip trigger circuit. High: -0.6V (max) to -0.8V (min). Low: -1.45V (max) -1.75V (min).

(iii) Check that the centre voltage of backlash at TR6 collector is between -2.05V and -2.35V

(iv) Select FREQUENCY mode, 10 mV sensitivity, stored display. Set output of Signal Generator Item 1.0.(d) terminated in 20 dB and 50 ohm load, to 80 MHz and 25 mV p-p amplitude. Amplitude check should be made using calibrated oscilloscope, item 1.0.(c). Connect to input A, check that by using LEVEL control stable, correct operation can be obtained.

(v) Repeat (iv) above, changing input to 99.9 MHz and 45 mV p-p.

(vi) Repeat (iv) above, changing input to 110 MHz and 60 mV p-p.

(vii) With 85 mV p-p input indicated (i.e. not corrected) determine and record approximate maximum frequency for stable operation.

(g) Time Base (Divider) Calibration

Model SM201

Connect 90 MHz output of frequency standard, item 1.0 (b) to input A. Select Range 3. Check that a display of 90.0000 MHz can be obtained within the centre 60% range of trimmer capacitor C.3. If not, alter value of C4.

Select Range 4 and adjust C3 to give a display of (over range) 0000.00 kHz, ± 2 bits.

Select Range 3, check that display is 90.0000 MHz ± less than 1 bit (as interpreted from reading of 90.0000/90.0001 or 90.0000/89.9999). This checks that the constant gate time error is less than 11 ns.

Model SM201H

Connect 90 MHz output of frequency standard, item 1.0 (b), to input A. Select Range 3. Check that by trimming oscillator X2, display may be set to 90.0000 MHz. Select range 5, adjust oscillator X2 to give display of (over range) 000.000 kHz, flickering ± 1 bit.

Select Range 4, check that display is (over range) 0000.00 ± less than 1 bit (as interpreted from reading of 0000.00/0000.01 or 0000.00/9999.99). This checks that constant gate time error is less than 11 ns.

NOTE The crystal element of oscillator X2 is in a temperature-controlled oven. At least 10 minutes warm-up must be allowed from switch on, before adjusting the oscillator.

(h) Average Period Mode

(i) Select average period, stored display, 10 mV sensitivity, Range 5. Apply 100 kHz output of frequency standard to input A. Check that display reads 10,000 us ± 1. Select range 6. Check that display reads (over range) 0.00000 μs ± 1.

(ii) Using Signal Generator, item 1.0. (e), apply 12.5 MHz signal of 9 mV r.m.s. (25 mV peak to peak). Adjust LEVEL control to approximate centre of the arc of stable display (approximately 0.08000 μs). Increase input amplitude steadily to 100 mV r.m.s. (300 mV peak to peak). Check that display is stable without adjustment of LEVEL control.

(j) Attenuator Tests

(i) *L.F. Tests*

Select AVERAGE PERIOD, 10 mV sensitivity, range 2. Apply 1 kHz signal from Signal Generator, item 1.0 (f). Determine minimum signal for stable display. Let this be V.min.

Select 100 mV	Minimum signal should now be 10 (V min) ± 10%
Select 1V	Minimum signal should now be 100 (V min) ± 10%
Select 10V	Minimum signal should now be 1000 (V min) ± 20%

(ii) *H.F. Tests*

Set input frequency to 1 MHz. Select Range 5.
Determine minimum signal for stable display (= V'min).

Select 100 mV	Minimum signal should now be 10 (V'min) −5%, +30%
Select 1V	Minimum signal should now be 100 (V'min) 0, +50%
Select 10V	Minimum signal should now be 1000 (V'min) −40%, +60%

(k) External Clock Tests

(i) Select EXTERNAL CLOCK, FREQUENCY, Range 3, 10 mV sensitivity . Connect 15 MHz signal, 1.2V peak to peak from signal generator item 1.0. (e), to the EXT. CLOCK terminals. Connect the 90 MHz output of Frequency Standard, item 1.0. (b) to input A. Check that a stable display of 06.0000 MHz approximately may be obtained.

(ii) Select Range 1. Connect 1 kHz signal, 1.2V peak to peak, from signal generator, item 1.0. (f) to the external clock terminals. Connect the 1 MHz output of frequency standard, Item 1.0. (b) to input A. Check that a stable display of 1000.00 MHz approximately can be obtained. Release EXTERNAL CLOCK.

(l) External Reset

(i) Select FREQUENCY, Range 1, 10 mV sensitivity. Apply signal (approximately 80 mV peak to peak, 100 MHz), to Channel A. Adjust for stable display. Apply d.c. voltage to EXTERNAL RESET input, monitored by Avometer. Check that with +0.85V applied, readings are inhibited and display is 0000.00 MHz. Check that with +1.15V applied, readings are allowed.

(ii) For EXTERNAL RESET input, use 1.4 kHz sinewave, 6V peak to peak (2.12V r.m.s.) from item 1.0 (f). Select HOLD. Check that display shows 0000.00 MHz and stable measurement of A input frequency, apparently simultaneously. There should be no miscounts.

(m) Period Mode

(i) Select PERIOD MODE, 10 mV sensitivity, Range 1. Also select PERIOD on PERIOD PULSE WIDTH toggle switch. Apply 100 Hz sinewave, 500 mV peak to peak from signal generator item 1.0 (g) to input A, giving a display of .010000 secs approximately. Adjust input frequency to give a convenient beat frequency with the internal ripple (say 1 Hz). Check that amplitude observed on display, due to the beat, is less than 10 bits peak-to-peak.

(ii) Select PULSE WIDTH −. Remove input signal. Check that gate opens as LEVEL control is moved clockwise through trigger point, and is closed for the reverse direction. Repeat for PULSE WIDTH +, operation should be reversed.

(iii) Select PERIOD on toggle switch, and Range 3. Apply 10 Hz sinewave, 25 mV peak to peak to input A. Check that a stable display may be obtained, with random noise less than 10 bits, peak-to-peak.

(iv) Apply 10 Hz square wave (approximately 1 : 1 mark-space ratio) 25 mV peak-to-peak to input A. Check that the instrument operates on PULSE WIDTH − and PULSE WIDTH +. Check, by using the LEVEL control , that the instrument can be triggered between the leading and trailing edges. Outside the operating range, rapid changes of reading will be seen, due to differentiation in the input amplifier.

(n) 'B' and 'C' Inputs

(i) Select TIME MODE, B−B, and Range 1. Apply 1 kHz sinewave, 0.3V peak-to-peak, +1V d.c. to input B, using Oscillator item 1.0 (g). Check satisfactory operation for POSITIVE and NEGATIVE positions of B

toggle switch. Reading should be .001000 seconds approximately.

(ii) Change input to 2 Hz sinewave, 2V peak-to-peak +1V d.c. Check satisfactory operation for POSITIVE and NEGATIVE positions of B toggle switch. Reading should be 0.5 seconds approximately.

(iii) Select B—C. Apply 1 kHz square wave, 0.3V peak-to-peak +1V d.c. to inputs B and C in parallel. Check satisfactory operation for B POSITIVE to C NEGATIVE, and B NEGATIVE to C POSITIVE.

(iv) Change B and C inputs to 1 kHz sinewave, approximately 2V peak-to-peak + 1V d.c. Check that, as d.c. level of input is changed towards zero, B POSITIVE to C NEGATIVE interval decreases, and B NEGATIVE to C POSITIVE interval increases.

(v) Change B and C inputs to 2 Hz sinewave, 2V peak-to-peak +1V d.c. Check satisfactory operation for B POSITIVE to C NEGATIVE and B NEGATIVE to C POSITIVE.

(p) Count Mode Operation

(i) Select COUNT MODE, Range 1, 10 mV sensitivity, B—B. Apply 500 Hz sinewave, approximately 4V peak-to-peak to input B, using Oscillator, item 1.0 (f). Apply 5 MHz output of frequency standard, item 1.0 (b) to input A. Check that display is 010000 approximately.

(ii) Select Range 2, leaving inputs as above. Check that display is divided by ten.

SECTION 6

PARTS LIST

1. INTRODUCTION

1.1 This section contains information for ordering replaceable parts. Tables 6.1 to 6.5 provide the following information:

(a) Circuit reference
(b) Description
(c) Manufacturer/reference
(d) S.E. Laboratories part number
(e) Value, tolerance and rating for each component

1.2 Minor items, such as screws, nuts, etc., have not been included as they are not considered special to the equipment.

2. ORDERING INFORMATION

2.1 When ordering your replacement part, address the order to your local agent, or to S.E. LABORATORIES, (Engineering) LTD., Service Department, North Feltham Trading Estate, Feltham, Middlesex, England. Telephone Number Feltham 1166/5876.

2.2 Specify the following information, for each part:—

(a) Model and serial number of the equipment
(b) Part number
(c) Circuit reference
(d) Description

2.3 To order a part not listed give the part number, description of the next higher assembly which is listed and a complete description of the part required.

2.4 The assemblies are listed as follows:—

TABLE	
6-1	Display and Logic Board, PL 31651
6-2	Input Amplifier, PL 29813
6-3	Display Logic
6-4	BCD Outputs Unit SM244, PL 31649
6-5	Power Supply, PL 29701

TABLE 6.1 DISPLAY AND LOGIC BOARD

PL 31651

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		CAPACITORS (FIXED) uF			
C1	CS30105	STC, PMA 0.22 M100	0.22	20	100V
C2	CS30271	Erie, 811T	0.1	+50, −25	18V
C4	CS 30910	Guest, KSN-2	S.O.T.	10	160V
C5	CS30375	Guest, KSN-2	390p	10	63V
C6	CS30893	Guest, KSN-2	820p	10	63V
C7	CS30314	Guest, KSN-2	220p	10	63V
C8	As C2				
C9	CS30102	Guest, KSN-2	47p	10	160V
C10	As C2				
C11	As C2				
C12	As C2				
C13	As C2				
C14	As C2				
C15	As C2				
C16	As C2				
C17	As C2				
C18	As C2				
C19	As C2				
C20	As C2				
C21	As C2				
C22	As C2				
C23	As C2				
C24	As C2				
C25	As C2				
C26	CS30342	Guest, KSN-2	100p	10	63V
C27	CS30912	Guest, KSN-2	33p	10	160V
C28	CS30077	Guest, KSN-2	68p	10	160V
C29	CS30566	Erie, 831T	0.01	−25, +50	25V
C30	As C29				
C31	As C29				
C32	CS30936	C.C.L., WD126S	1000	+100, −20	
C33	CS30271	Erie, 811T	0.1	+50, −25	
		CAPACITORS (VARIABLE)			
C3	CS30901	Steatite, 10S Triko 06 3/10 No 33	3p−10p		250V
		DIODES			
D1	BS2045	Transitron, 1N914			
D2	As D1				
D3	BS2879	Mullard, 1N4009			
D4	As D3				
D5	As D3				

Table 6.1 (Cont.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
D6	As D3				
D7	As D3				
D8	As D1				
D9	As D1				
D10	As D3				
D11	As D3				
D12	As D3				
D13	As D3				
D14	As D3				
D15	As D3				
D16	As D1				
D17	As D3				
D18	As D3				
D19	As D3				
D20	As D3				
D21	As D3				
D22	As D3				
D23	BS2633	Texas IN2069			
D24	As D23				
		INTEGRATED CIRCUITS			
IC1	BS7400	Texas, 7400N			
IC2	As IC1				
IC3	As IC1				
IC4	As IC1				
IC5	BS7410	Texas, SN7410N			
IC6	As IC5				
IC7	BS7440	Texas, SN7440N			
IC8	As IC1				
IC9	As IC1				
IC10	BS7453	Texas, SN7453N			
IC11	BS7460	Texas, SN7460N			
IC12	As IC1				
IC13	As IC1				
IC14	As IC1				
IC15	As IC1				
IC16	As IC10				
IC17	As IC1				
IC18	BS7473	Texas, SN7473N			
IC19	As IC18				
IC20	As IC18				
IC21	AS IC18				
IC22	As IC18				
IC23	BS7490	Texas, SN7490N			
IC24	As IC23				
IC25	As IC23				

Table 6.1 (Cont.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
IC26	As IC23				
IC27	As IC23				
IC28	As IC23				
IC29	As IC23				
IC48	As IC1				
IC49	As IC23				
		RESISTORS (FIXED) Ω			
R1	DS5636	Morganite, XL	2.2k	10	¼W
R2	DS7256	Electrosil, TR4	510	5	
R3	As R2				
R4	DS7270	Electrosil, TR4	1.5k	5	
R5	As R1				
R6	DS6348	Morganite, XL	3.9k	10	¼W
R7	As R6				
R8					
R9	DS5981	Morganite, XL	39k	10	¼W
R10	As R2				
R11	As R2				
R12	As R4				
R13	As R1				
R14	DS5966	Morganite, XL	33k	10	¼W
R15	DS7415	Morganite, XL	1.5k	10	¼W
R16	As R2				
R17	As R2				
R18	As R4				
R19	As R15				
R20	DS32216	Morganite, XL	270	10	¼W
R21	DS7430	Morganite, XL	47k	10	¼W
R22	As R1				
R23	DS6725	Morganite, XL	47	10	¼W
R24	DS7315	Morganite, XL	22	10	¼W
R25	As R2				
R26	As R2				
R27	As R4				
R28	As R2				
R29	As R2				
R30	As R4				
R31	DS5739	Morganite, XL	4.7k	10	¼W
R32	DS6090	Morganite, XL	100k	10	¼W
R33	As R14				
R34	As R15				
R35					

Table 6.1 (Cont.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R36	As R1				
R37	As R21				
R38	DS7315	Morganite, XL	22	10	¼W
R39	DS33520	Electrosil, TR4	240	5	
R40	DS6506	Electrosil, TR4	2.2k	5	
R41	As R15				
R42					
R43	As R14				
R44	As R21				
R45	As R15				
R46	As R15				
R47	As R15				
R48	As R15				
R49					
R50	As R9				
R51	DS 5465	Morganite, XL	470	10	¼W
R52	DS6352	Morganite, XL	560	10	¼W
R59	DS5927	Morganite, XL	2 2k	10	¼W
R60	DS33148	Morganite, XL	2 2k	10	¼W
R61	As R60				
R62					
R63	As R59				
R64	DS5848	Morganiate, XL	10k	10	¼W
		TRANSISTORS			
TR1	BS2737	Mullard, BFY52			
TR2	BS2599	Mullard, BSX20			
TR3	As TR2				
TR4	BS2845	Mullard, BSX21			
TR5	As TR2				
TR6	As TR2				
TR7	As TR2				
TR8					
TR9	As TR2				
TR10	As TR2				
TR11	As TR2				
TR12	As TR2				
TR13	As TR2				

Table 6.1 (Cont.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
TR14	As TR4				
TR15	As TR2				
TR16	As TR2				
TR17	As TR2				
TR18	As TR2				
		MISCELLANEOUS			
SW1	QS22291	Toggle switch, D.P.D.T. Waycom, MST205TA			
SW2	As SW1				
SW3	QS22292	Toggle switch, D.P.D.T. Waycom, MST205PA			
–	D29937	7-push-button switch bank			
–	D29938	10-push-button switch bank			
–	B29947	Switch P.C.Board			
ILP1	JS14070	Neon, West Hyde Dev. type Q, 240V.			
ILP2	As ILP1				
SKTB	As 1442	Socket, co-axial, BNC P.E.T. 742/PTFE/MOD SEL.			
SKTC	As SKT -B				
X1	WS28589	Crystal, 2MHz, Crystal Électronics, MD		0.005	
X2	WS28724	Oscillator, Cathodeon FS 5951/01			
SKTD	AS 1434	Terminal socket (fixed) Belling Lee, L1717 (Red)			
SKTE	As SKTD				
SKTF	AS 1435	Terminal socket (fixed) Belling Lee, L1717 (Black)			
		Mating Plugs for above			
–	AS 0459	Terminal plug (free) L1716 (Red)			
–	AS 0460	Terminal plug (free) L1716 (Black)			

TABLE 6.2 **INPUT AMPLIFIER** **PL 29813**

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		CAPACITORS (FIXED) uF			
C1	CS 30271	Erie, 811T	0.1	–25, +50	18V
C2	CS 30898	Erie, P100/YD	2.2p	0.5	30V
C3	CS 30314	Guest, KSN-2	220p	10	63V
C4	CS 30900	Erie, K120051/YD/470	470p	10	200V
C5	As C1				
C6	As C1				
C7	CS 30631	Mullard, C426AR/C200	200		6.4V
C8	CS 30177	Erie, 831/K350081	1000p	20	500V
C9	As C8				
C10	CS 30895	Erie, P100/YD	4.7p	±0.5p	200V
C11	As C10				
C12	CS 30449	Erie, 831	470p	20	500V
C13	As C1				
C14	As C8				
C15	CS 30225	Mullard, C426AR/B64	64		4V
C16	As C1				
C17	As C1				
C18					
C19	CS 30566	Erie, 831T	0.01	–25, +50	25V
C20	As C19				
C21	As C19				
C22	As C1				
C23	As C1				
		DIODES			
D1	BS 2045	1N 914, or 1N 4009 (St. No. BS 2879)			
D2	As D1				
D3	As D1				
		INTEGRATED CIRCUITS			
IC1	BS 2884	Motorola, MC 1013P			
IC2	As IC1				
IC3	As IC2				
IC4	As IC3				
IC5	BS 2883	Motorola, MC 1014P			
IC6	BS 2880	Motorola, MC 1027P			
IC7	As IC1				
IC8	BS 2885	Motorola, MC 1010P			
IC9	As IC8				
IC10	BS 2882	RCA, CA 3046			

TABLE 6.2 (Cont.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		RESISTORS (FIXED) Ω			
R1	DS 6082	Dubilier, BTT	100k	5	½W
R2	DS 7235	Morganite, XL	1M	10	¼W
R3	DS 7415	Morganite, XL	1.5k	10	¼W
R4					
R5	DS 6524	Morganite, XL	15	10	¼W
R6	DS 33503	Electrosil, TR4	750	1	
R7	DS 33504	Electrosil, TR4	1.2k	2	
R8	DS 33505	Electrosil, TR4	680	1	
R9	DS 33506	Electrosil, TR4	620	1	
R10	As R5				
R11	As R5				
R12	DS 33507	Electrosil, TR4	200	1	
R13	As R6				
R14					
R15	As R6				
R16	DS 33508	Electrosil, TR4	470	1	
R17	DS 33509	Electrosil, TR4	16k	1	
R18	DS 33510	Electrosil, TR4	22k	1	
R19	DS 7329	Morganite, XL	10M	5	¼W
R20	DS 32789	Morganite, XL	560k	10	¼W
R21					
R22	DS 7237	Morganite, XL	56k	10	¼W
R23	DS 33502	Electrosil, TR4	1k	2	
R24	As R22				
R25	DS 32231	Morganite, XL	390	10	¼W
R26	DS 32626	Morganite, XL	150k	10	¼W
R27	DS 33501	Morganite, XL	27	10	¼W
R28	DS 33511	Electrosil, TR4	330	1	
R29	DS 33512	Electrosil, TR4	160	1	
R30	DS 5085	Morganite, XL	12	10	¼W
R31	As R29				
R32	As R23				
R33	DS 33513	Electrosil, TR4	82	1	
R34	DS 33514	Electrosil, TR4	820	1	
R35	DS 33515	Electrosil, TR4	110	5	
R36	DS 33516	Electrosil, TR4	270	1	
R37	DS 33517	Electrosil, TR4	1.5k	1	
R38	DS 7315	Morganite, XL	22	10	¼W
R39	DS 5465	Morganite, XL	470	10	¼W
R40	DS 6358	Morganite, XL	1k	10	¼W
R41	DS 7235	Morganite, XL	1M	10	¼W
R42	DS 5075	Morganite, XL	10	10	¼W

TABLE 6.2 (Cont.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		TRANSISTORS			
TR1	BS 2881	R.C.A., 3N 138			
TR2	BS 2835	R.C.A., 2N 5179			
TR3	BS 2839	R.C.A., 40235			
TR4	AS TR2				
TR5	AS TR1				
TR6	BS 2838	Motorola, MPS 3640			
TR7	As TR6				
TR8	As TR2				
TR9	As TR2				
TR10	As TR3				
		MISCELLANEOUS			
X1	GS 11197	Ferroxcube bead, Mullard, FX 1115			
X2	As X1				
SW4	D 31657	Switch, A.B. Metals			
C1	CS 30902	Erie, N750/XD	3.3p	±0.25p	750V
C2	CS 30925	Erie, P100XD	2.4p	±0.25p	750V
C3	CS 30396	Guest, KSN-2	22p	10	160V
C4	CS 4299	Waycom, Tropyfol F.	0.1	10	400V
R1	DS 5075	Morganite, XL	10	10	¼W
R2	DS 7315	Morganite, XL	22	10	¼W
R3	As R2 (above)				
R4	DS 7767	Radio Resistor, 2LCA 0309	910k	5	¼W
R5	DS 7976	Electrosil, TR4	110k	5	
R6	DS 74907	Radio Resistor, 2LCA 0309	1M	5	¼W
R7	DS 6714	Electrosil, TR5	10k	5	
RV1	FS 10429	Resistor, variable, linear, Reliance, CWO5	10k	10	
SKT A	AS 1442	Socket, co-axial, BNC P.E.T. 742/PTFE/MOD.SEL.			

TABLE 6.3 DISPLAY LOGIC

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		INTEGRATED CIRCUITS			
IC30	BS7541	Texas, SN74141			
IC31	As IC30				
IC32	As IC30				
IC33	As IC30				
IC34	As IC30				
IC35	As IC30				
IC36	BS7475	Texas, SN7475N			
IC37	As IC30				
IC38	As IC30				
IC39	As IC30				
IC40	As IC30				
IC41	As IC30				
IC42	BS7490	Texas, SN7490N			
IC43	As IC42				
IC44	As IC42				
IC45	As IC42				
IC46	As IC42				
IC47	BS7450	Texas, SN7450N			
		DISPLAY TUBES			
V1	WS28677	Mullard, ZM1174			
V2	As V1				
V3	As V1				
V4	As V1				
V5	As V1				
V6	As V1				

TABLE 6.4 BCD OUTPUTS UNIT SM 244

PL 31649

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		CAPACITORS (FIXED) uF			
C1	CS30271	Erie, 811T	0.1	+50, −25	18V
C2	As C1				
C3	As C1				
		DIODES			
D1	BS2525	Mullard, BZY88 C6V2			
D2	BS2828	Texas 1N914			
		INTEGRATED CIRCUITS			
IC1	BS7400	Texas, SN7400N			
IC2	BS7404	Texas, SN7404N			
IC3	As IC2				
IC4	As IC2				
IC5	As IC2				
IC6	As IC2				
IC7	As IC2				
IC8	As IC2				
IC9	As IC2				
		MISCELLANEOUS			
FS1	RS23125	Fuse link, 250mA, Bulgin, F290/.250A			
—	AS 1460	Socket, 34-way, McMurdo, MS 134			
—	AS 500	Plug, 34-way, McMurdo, MP 134			

TABLE 6.5 POWER SUPPLY

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
		CAPACITORS (FIXED) uF			
C1					
C2	CS30274	Mullard, C437AR/F250	250		25V
C3	CS30343	Erie, 811/T/30	0.1	+50, −25	30V
C4	As C3				
C5	As C3				
C6	As C3				
C7	CS30891	Erie, KA3051K	6,800		16V
C8	CS30892	Mullard, C431BR/E2000	2000		16V
		DIODES			
D1	BS2522	Mullard, BYX10			
D2	BS2579	Texas, 1S130			
D3	BS2633	Texas, 1N2069			
D4	As D3				
D5	As D2				
D6	As D2				
D(Z)7	BS2695	Mullard, BZY88/C3V9			
D8	BS2045	1N914			
D9	As D8				
		INTEGRATED CIRCUITS			
IC1	BS2882	R.C.A., CA 3046			
		RESISTORS (FIXED) Ω			
R1	DS32267	Morganite, XL	220k	10	¼W
R2	DS5075	Morganite, XL	10	10	¼W
R3	DS32177	Electrosil, TR6	47	5	
R4	DS7234	Morganite, XL	1.8k	10	¼W
R5	DS33518	Electrosil, TR4	5.1k	1	
R6	DS33519	Electrosil, TR4	2.2k	1	
R7	DS5571	Morganite, XL	1.2k	10	¼W
R8	DS7301	Morganite, XL	5.6k	10	¼W
R9	DS5465	Morganite, XL	470	10	¼W
R10	DS5945	Morganite, XL	27k	10	¼W
R11	DS5739	Morganite, XL	4.7k	10	¼W
R12	DS33448	Morganite, XL	120k	10	¼W
R13	DS6924	Electrosil, TR4	1k	5	
R14	DS6841	Electrosil, TR4	2.7k	5	
R15	DS32784	Electrosil, TR4	6.8k	1	
R16	As R15				

Table 6.5 (Cont.)

Cct. Ref.	S.E.L. Part No.	Manufacturer/Reference	Value	Tol ± %	Rating
R17	DS7583	Morganite, XL	33	10	¼W
R18	DS6596	Electrosil, TR4	470	5	
		RESISTORS (VARIABLE) Ω			
RV1	FS10347	Reliance, CW52	1k		
		TRANSISTORS			
TR1	BS2781	Mullard, BFX88			
TR2	BS2737	Mullard, BFY52			
TR3	BS2519	Mullard, BCY72			
TR4	As TR2				
TR5	BS2352	R.C.A., 2N3055			
		MISCELLANEOUS			
FS1	RS23058	Fuse link, 200mA, Beswick, TDC123			
T1	ES8415	Transformer, D2650 Ripley TFR, 5/387			
SW5	QS22230	Toggle switch, Painton 22/10/0201/00			
–	ES8377	Choke, Buckingham Electronics, BE69323			

SECTION 7

CIRCUIT AND COMPONENT LAYOUT DIAGRAMS.

FIG. 1 TIMER COUNTER SM201 — CIRCUIT DIAGRAM E31341/6
(SHT. A FREQUENCY MODE)

NOTES

1. NUMBERS ON POLES, THUS o5 DENOTES CONNECTIONS TO DECIMAL POINTS, NUMBERED FROM LEFT TO RIGHT ON DISPLAY.
2. CAPACITORS C10 TO C25 INCLUSIVE ARE CONNECTED BETWEEN 0V AND +5V ACROSS INTEGRATED CIRCUITS.
3. WITH HIGH STAB. OSC. FITTED (SM201H) CRYSTAL X1 IS NOT FITTED. WITH STANDARD OSC. FITTED CRYL X2 AND IC's 48 AND 49 ARE NOT FITTED.
4. ◉ DENOTES WIRING PIN.
   ▭ DENOTES SOLDERED PLUG-IN PIN.

EXTERNAL CLOCK INPUT AMPLIFIER

HIGH STABILITY CLOCK OSCILLATOR (SM201H ONLY) (SEE NOTE 3)

CLOCK OSCILLATOR (STANDARD)

POLARITY SELECTION GATES

RANGE SELECTION GATES

TO DISPLAY CIRCUIT B31133

SEE NOTE 1

POWER SUPPLY (PIN 5 ON B29691)

RESET
EXTERNAL CLOCK
HOLD
B-C
B-B
TIME SECS.
AVERAGE PERIOD μ SECS
PERIOD A SECS
FREQ A
COUNT A
KHz 10⁵
KHz 10⁴
KHz 10³
MHz 10²
MHz 10
MHz 1
NON. STORED

FIG. 1 TIMER COUNTER SM201 – CIRCUIT DIAGRAM E31341/6

(SHT. B PERIOD & PULSEWIDTH MODE.)

EXTERNAL CLOCK INPUT AMPLIFIER

MAINS TRANSFORMER SEE DWG B29691

HIGH STABILITY CLOCK OSCILLATOR (SM201H ONLY) (SEE NOTE 3)

CLOCK OSCILLATOR (STANDARD)

POLARITY SELECTION GATES

RANGE SELECTION GATES

6TH DECADE COUNTER (IC42, PIN 11)

TO DISPLAY CIRCUIT B31133

SEE NOTE 1

NOTES

1. NUMBERS ON POLES, THUS o5 DENOTES CONNECTIONS TO DECIMAL POINTS, NUMBERED FROM LEFT TO RIGHT ON DISPLAY.
2. CAPACITORS C10 TO C25 INCLUSIVE ARE CONNECTED BETWEEN 0V AND +5V ACROSS INTEGRATED CIRCUITS.
3. WITH HIGH STAB. OSC. FITTED (SH201H) CRYSTAL X1 IS NOT FITTED. WITH STANDARD OSC. FITTED CRYL X2 AND IC's 48 AND 49 ARE NOT FITTED.
4. ◉ DENOTES WIRING PIN.
   — DENOTES SOLDERED PLUG-IN PIN.

BOARD TRACKING (SEE DWG. B31133)

STORE GATE PULSE (MAIN COUNTER STORES PINS 4 & 13)

COUNTER RESET

OVER RANGE (PIN 27 BCD OUTPUT BOARD D31664)

OVER RANGE

GATE OPEN

PULSE WIDTH

PERIOD

POWER SUPPLY (PIN 5 ON B29691)

RESET

EXTERNAL CLOCK

HOLD

B-C

B-B

TIME SECS.

AVERAGE PERIOD μ SECS.

PERIOD A SECS.

FREQ. A

COUNT A

KHz 10^5

KHz 10^4

KHz 10^3

MHz 10^2

MHz 10

MHz 1

NON. STORED

FIG. 1 TIMER COUNTER SM201 – CIRCUIT DIAGRAM E31341/6
(SHT. C AVERAGE PERIOD MODE)

EXTERNAL CLOCK INPUT AMPLIFIER

MAINS TRANSFORMER SEE DWG B29691

HIGH STABILITY CLOCK OSCILLATOR (SM201H ONLY) (SEE NOTE 3)

CLOCK OSCILLATOR (STANDARD)

6TH DECADE COUNTER (IC42, PIN 11)

TO DISPLAY CIRCUIT B31133

POLARITY SELECTION GATES

RANGE SELECTION GATES

POWER SUPPLY (PIN 5 ON B29691)

BOARD TRACKING (SEE DWG. B31133)

STORE GATE PULSE (MAIN COUNTER STORES PINS 4 & 13)

COUNTER RESET

OVER RANGE (PIN 27 BCD OUTPUT BOARD D31664)

NOTES

1. NUMBERS ON POLES, THUS o5 DENOTES CONNECTIONS TO DECIMAL POINTS, NUMBERED FROM LEFT TO RIGHT ON DISPLAY.
2. CAPACITORS C10 TO C25 INCLUSIVE ARE CONNECTED BETWEEN 0V AND +5V ACROSS INTEGRATED CIRCUITS.
3. WITH HIGH STAB. OSC. FITTED (SM201H) CRYSTAL X1 IS NOT FITTED. WITH STANDARD OSC. FITTED CRYL X2 AND IC's 48 AND 49 ARE NOT FITTED.
4. ◉ DENOTES WIRING PIN.
   — DENOTES SOLDERED PLUG-IN PIN.

FIG. 1 TIMER COUNTER SM201 — CIRCUIT DIAGRAM E31341/6

(SHT. D TIME MODE)

NOTES

1. NUMBERS ON POLES, THUS o5 DENOTES CONNECTIONS TO DECIMAL POINTS, NUMBERED FROM LEFT TO RIGHT ON DISPLAY.
2. CAPACITORS C10 TO C25 INCLUSIVE ARE CONNECTED BETWEEN 0V AND +5V ACROSS INTEGRATED CIRCUITS.
3. WITH HIGH STAB. OSC. FITTED (SM201H) CRYSTAL X1 IS NOT FITTED. WITH STANDARD OSC. FITTED CRYL X2 AND IC's 48 AND 49 ARE NOT FITTED.
4. ◉ DENOTES WIRING PIN.
   ⊖ DENOTES SOLDERED PLUG-IN PIN.

EXTERNAL CLOCK INPUT AMPLIFIER

HIGH STABILITY CLOCK OSCILLATOR (SM201H ONLY) (SEE NOTE 3)

CLOCK OSCILLATOR (STANDARD)

POLARITY SELECTION GATES

RANGE SELECTION GATES

6TH DECADE COUNTER (IC42, PIN 11)

TO DISPLAY CIRCUIT B31133

POWER SUPPLY (PIN 5 ON B29691)

RESET

EXTERNAL CLOCK

HOLD

B~C

B~B

TIME SECS.

AVERAGE PERIOD μ SECS.

PERIOD A SECS

FREQ A

COUNT A

KHz 10^5

KHz 10^4

KHz 10^3

MHz 10^2

MHz 10^1

MHz 1

NON. STORED

FIG. 1 TIMER COUNTER SM201 – CIRCUIT DIAGRAM E31341/6

(SHT. E COUNT MODE)

NOTES

1. NUMBERS ON POLES, THUS o5 DENOTES CONNECTIONS TO DECIMAL POINTS, NUMBERED FROM LEFT TO RIGHT ON DISPLAY.
2. CAPACITORS C10 TO C25 INCLUSIVE ARE CONNECTED BETWEEN OV AND +5V ACROSS INTEGRATED CIRCUITS.
3. WITH HIGH STAB. OSC. FITTED (SH201H) CRYSTAL X1 IS NOT FITTED. WITH STANDARD OSC. FITTED CRYL X2 AND IC's 48 AND 49 ARE NOT FITTED.
4. ◉ DENOTES WIRING PIN.
   ⇨ DENOTES SOLDERED PLUG-IN PIN.

BOARD TRACKING (SEE DWG. B31133)

- STORE GATE PULSE (MAIN COUNTER STORES PINS 4 & 13)
- COUNTER RESET

EXTERNAL CLOCK INPUT AMPLIFIER

MAINS TRANSFORMER SEE DWG B29691

HIGH STABILITY CLOCK OSCILLATOR (SM201H ONLY) (SEE NOTE 3)

CLOCK OSCILLATOR (STANDARD)

6TH DECADE COUNTER (IC42, PIN 11) SEE B3133

TO DISPLAY CIRCUIT B31133

POLARITY SELECTION GATES

RANGE SELECTION GATES

POWER SUPPLY (PIN 5 ON B29691)

OVER RANGE (PIN 27 BCD OUTPUT BOARD D31664)

GATE OPEN

PULSE WIDTH

PERIOD

RESET

EXTERNAL CLOCK

HOLD

B-C

B-B

TIME SECS

AVERAGE PERIOD μ SECS

PERIOD A SECS

FREQ A

COUNT A

KHz 10^5

KHz 10^4

KHz 10^3

MHz 10^2

MHz 10

MHz 1

NON STORED

FIG. 1 TIMER COUNTER SM201 – CIRCUIT DIAGRAM E31341/6

(SHT. F CONTROL LOGIC OPERATION)

NOTES

1. NUMBERS ON POLES, THUS o5 DENOTES CONNECTIONS TO DECIMAL POINTS, NUMBERED FROM LEFT TO RIGHT ON DISPLAY.
2. CAPACITORS C10 TO C25 INCLUSIVE ARE CONNECTED BETWEEN 0V AND +5V ACROSS INTEGRATED CIRCUITS
3. WITH HIGH STAB. OSC. FITTED (SM201H) CRYSTAL X1 IS NOT FITTED. WITH STANDARD OSC. FITTED CRYL X2 AND IC's 48 AND 49 ARE NOT FITTED.
4. ◉ DENOTES WIRING PIN.
   —○— DENOTES SOLDERED PLUG-IN PIN.

EXTERNAL CLOCK INPUT AMPLIFIER

CLOCK OSCILLATOR (STANDARD)

HIGH STABILITY CLOCK OSCILLATOR (SM201H ONLY) (SEE NOTE 3)

MAINS TRANSFORMER SEE DWG B29691

POLARITY SELECTION GATES

RANGE SELECTION GATES

6TH DECADE COUNTER (IC42, PIN 11)

BOARD TRACKING (SEE DWG B31133)

STORE GATE PULSE (MAIN COUNTER STORES PINS 4 & 13)

COUNTER RESET

TO DISPLAY CIRCUIT B31133

SEE NOTE 1

TO DISPLAY CIRCUIT B31133

POWER SUPPLY (PIN 5 ON B29691)

RESET (TO INPUT AMP.)

OVER RANGE (PIN 27 BCD OUTPUT BOARD D31664)

POINT A

BCD Bd

GATE OPEN

PULSE WIDTH

PERIOD

RESET

EXTERNAL CLOCK

HOLD

B-C

B-B

TIME SECS.

AVERAGE PERIOD μ SECS

PERIOD A SECS.

FREQ A

COUNT A

KHz 10^5

KHz 10^4

KHz 10^3

MHz 10^2

MHz 10

MHz 1

NON STORED

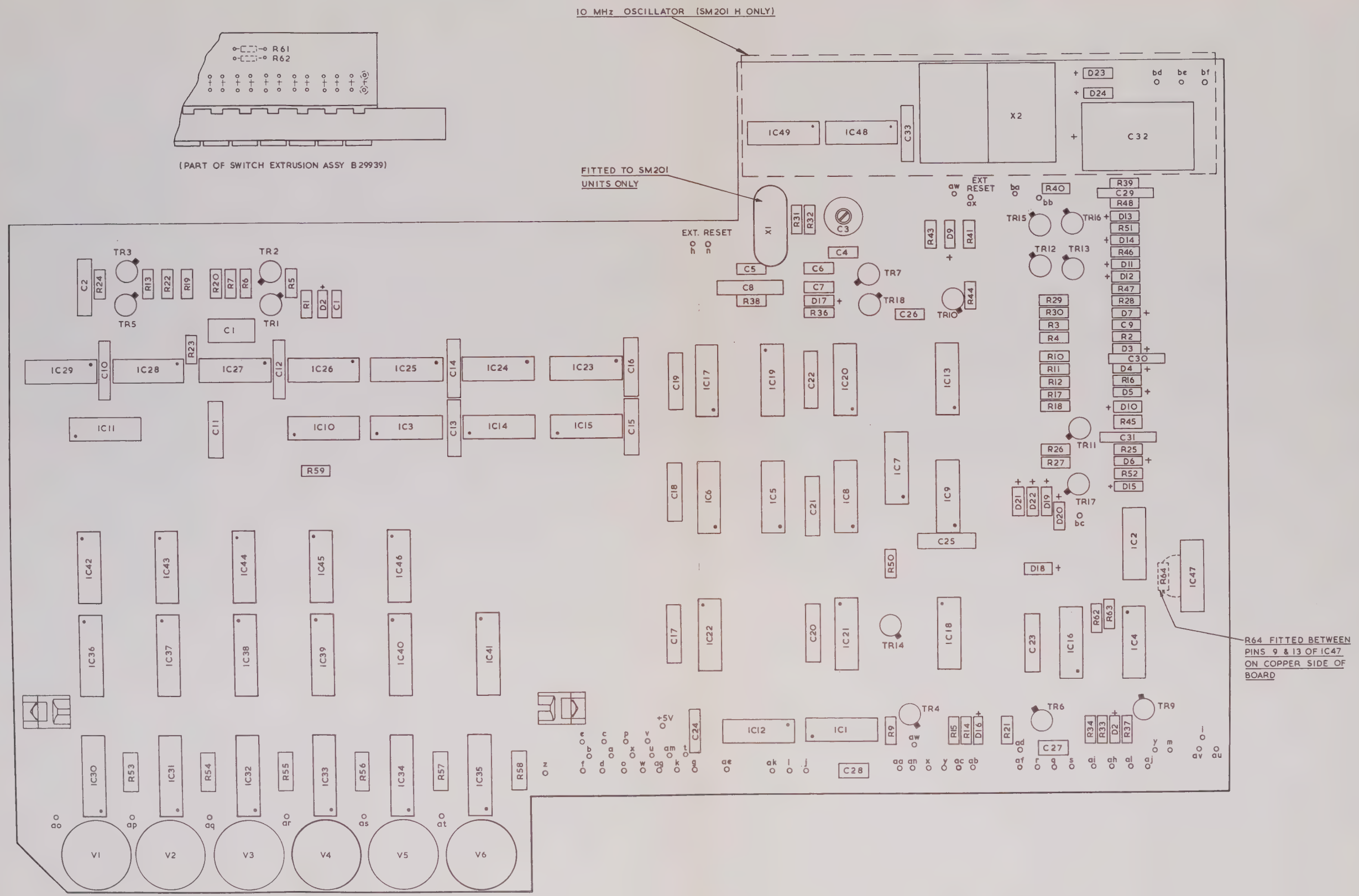
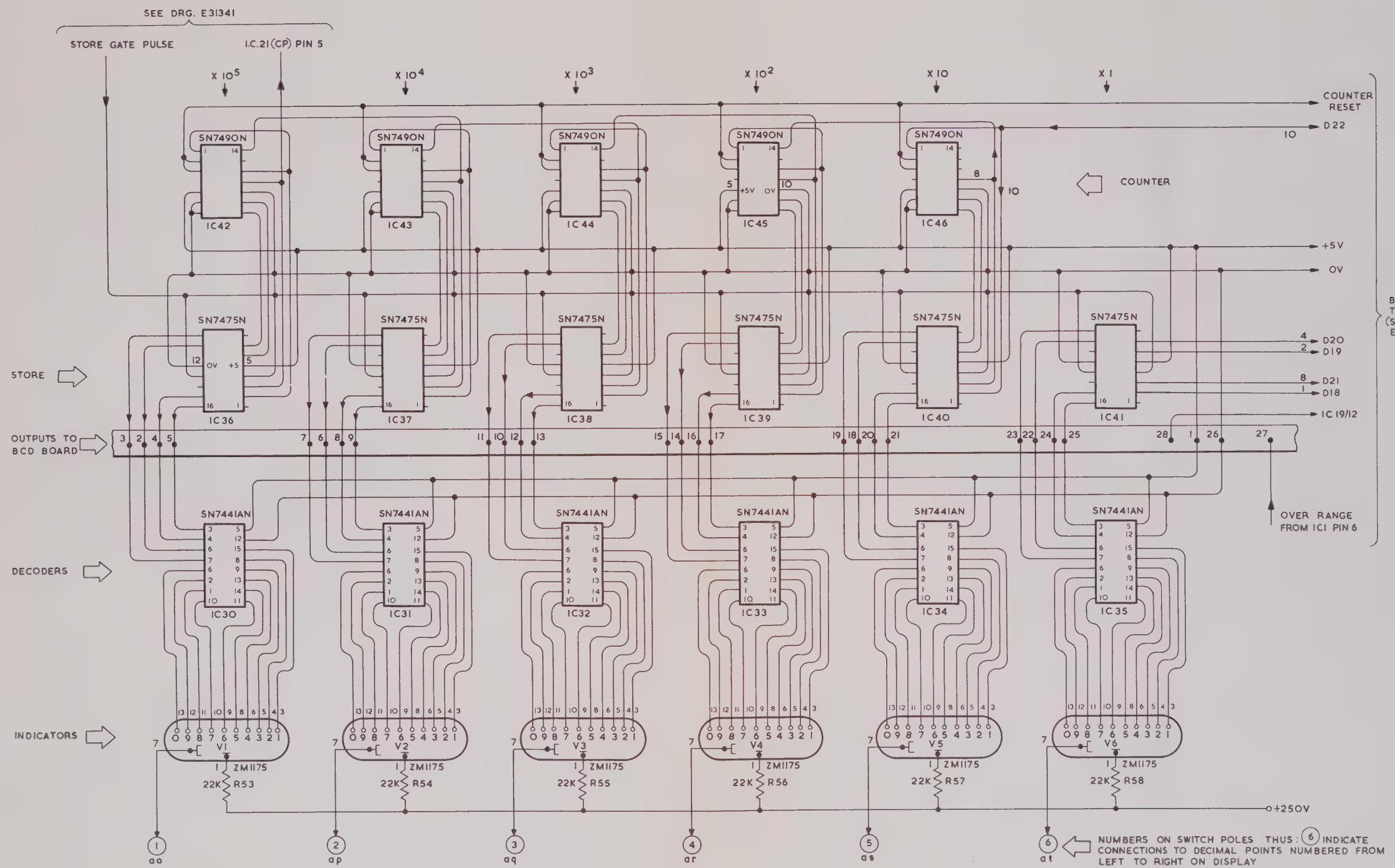
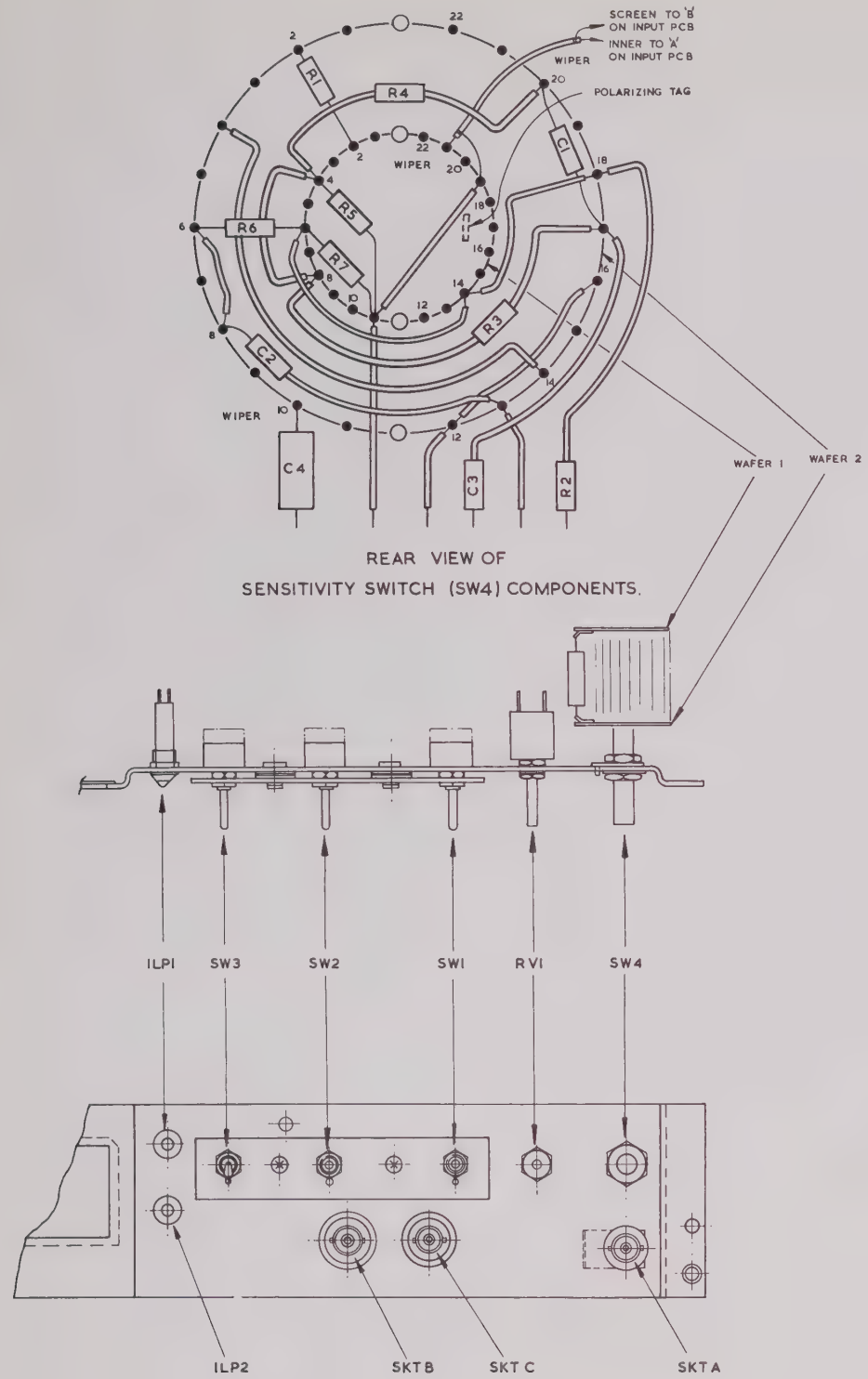


FIG. 2 DISPLAY & LOGIC BOARD – COMPONENT LAYOUT E.31651/52/53/5

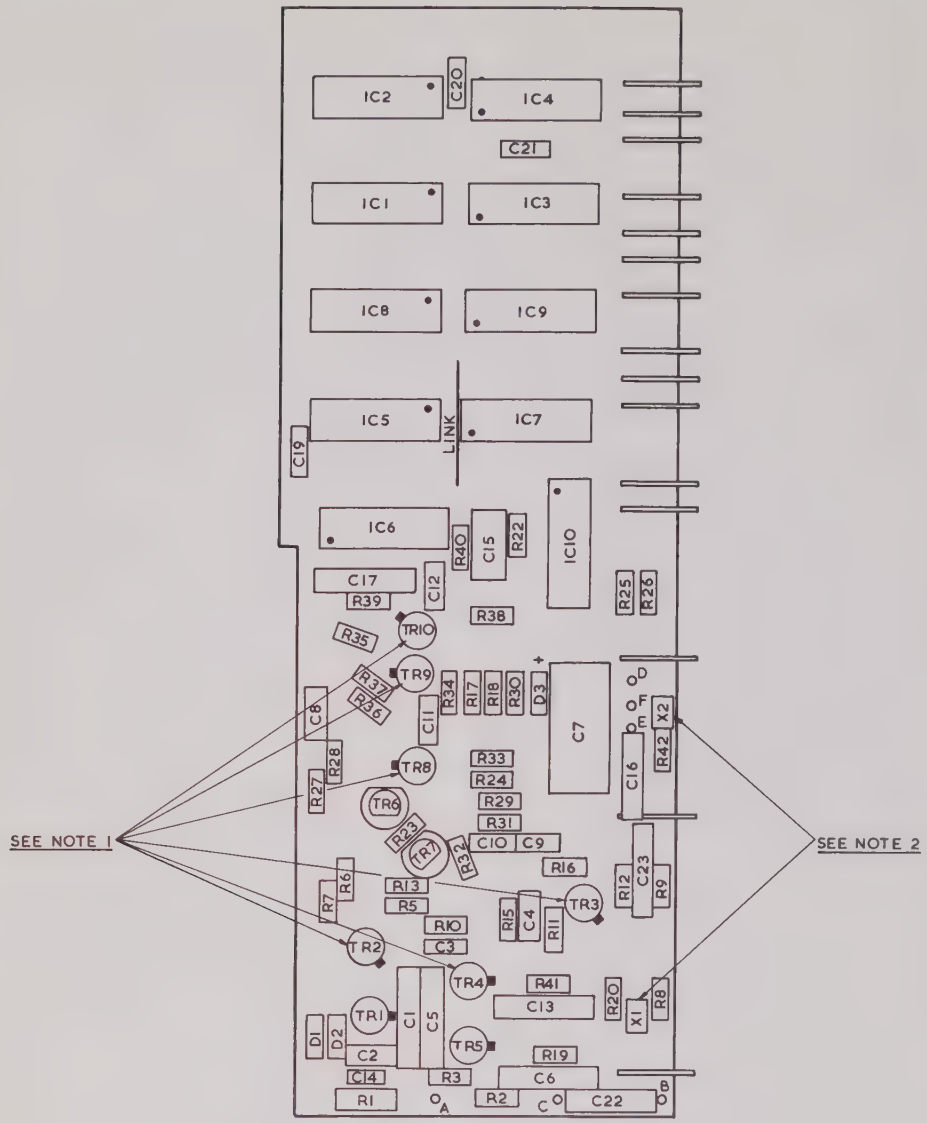
FIG 3 DISPLAY
CIRCUIT DIAGRAM B.31133/3





REAR VIEW OF
SENSITIVITY SWITCH (SW4) COMPONENTS.

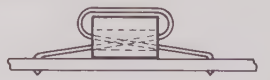
FIG. 4 FRONT PANEL- COMPONENT LAYOUT B 29855/2



NOTES

1. TRANSISTORS TR2, 3, 4, 8, 9 AND 10 INCLUSIVE TO HAVE 'CASE' LEAD CUT AS SHOWN BELOW

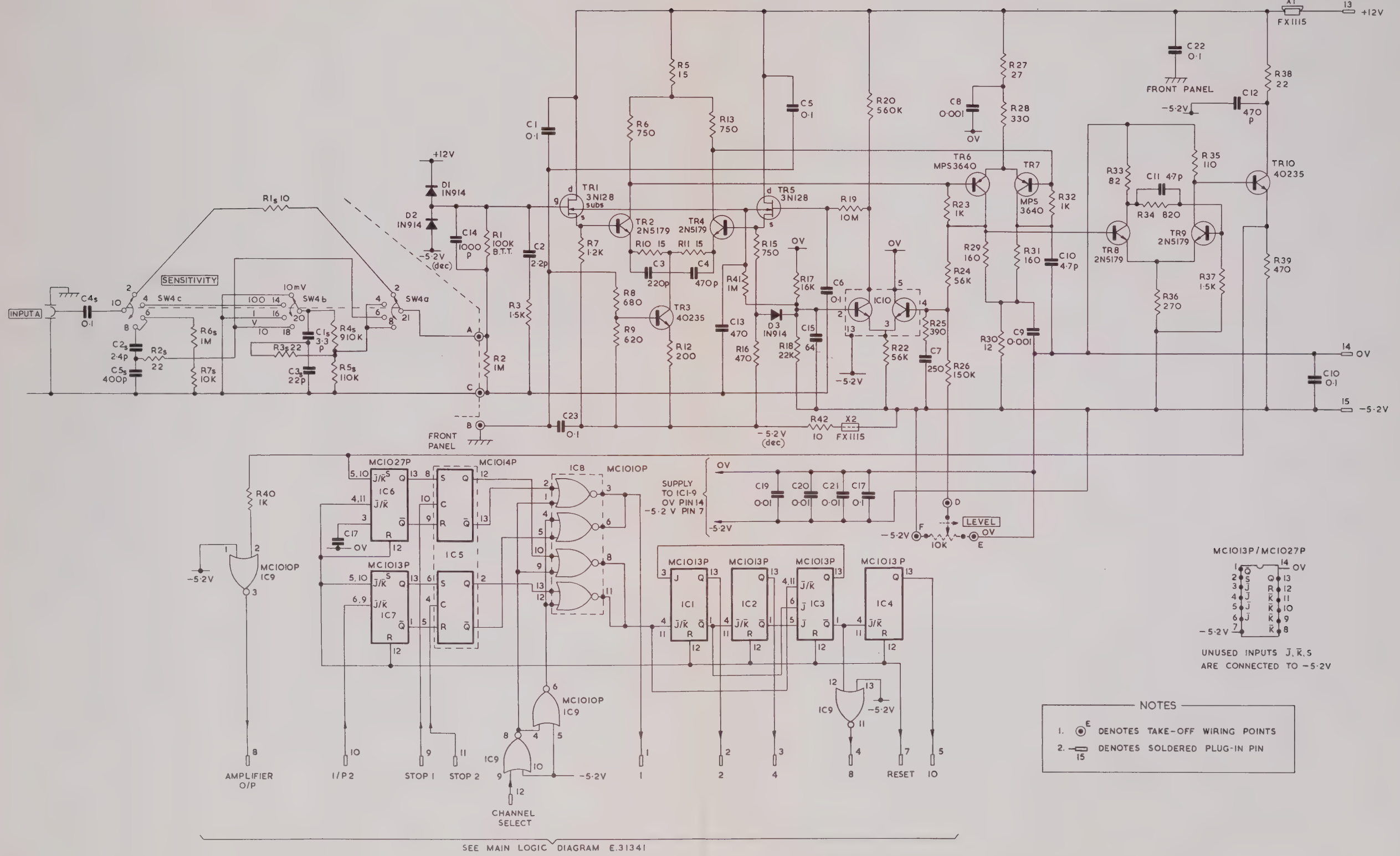
2(a) ASSEMBLE AND MOUNT FERRITE BEAD X1 AS SHOWN BELOW:



2(b) FERRITE BEADS X1 & X2 ARE INSULATED WITH 1 1/4" in WRAPS OF GLASS CLOTH TAPE.

FIG. 5. INPUT AMPLIFIER BOARD- COMPONENT LAYOUT B. 29813/2

FIG.6 INPUT AMPLIFIER CIRCUIT DIAGRAM B29814/2



MC1013P/MC1027P

UNUSED INPUTS J, $\overline{K}$, S ARE CONNECTED TO −5·2V

NOTES

1. ⊙ E DENOTES TAKE-OFF WIRING POINTS
2. —▭— 15 DENOTES SOLDERED PLUG-IN PIN

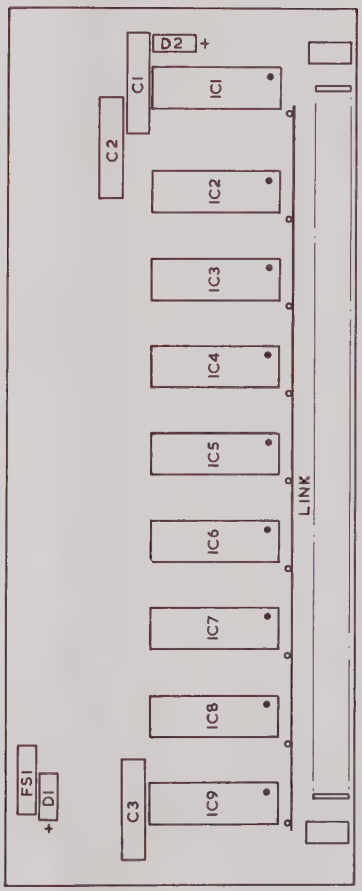
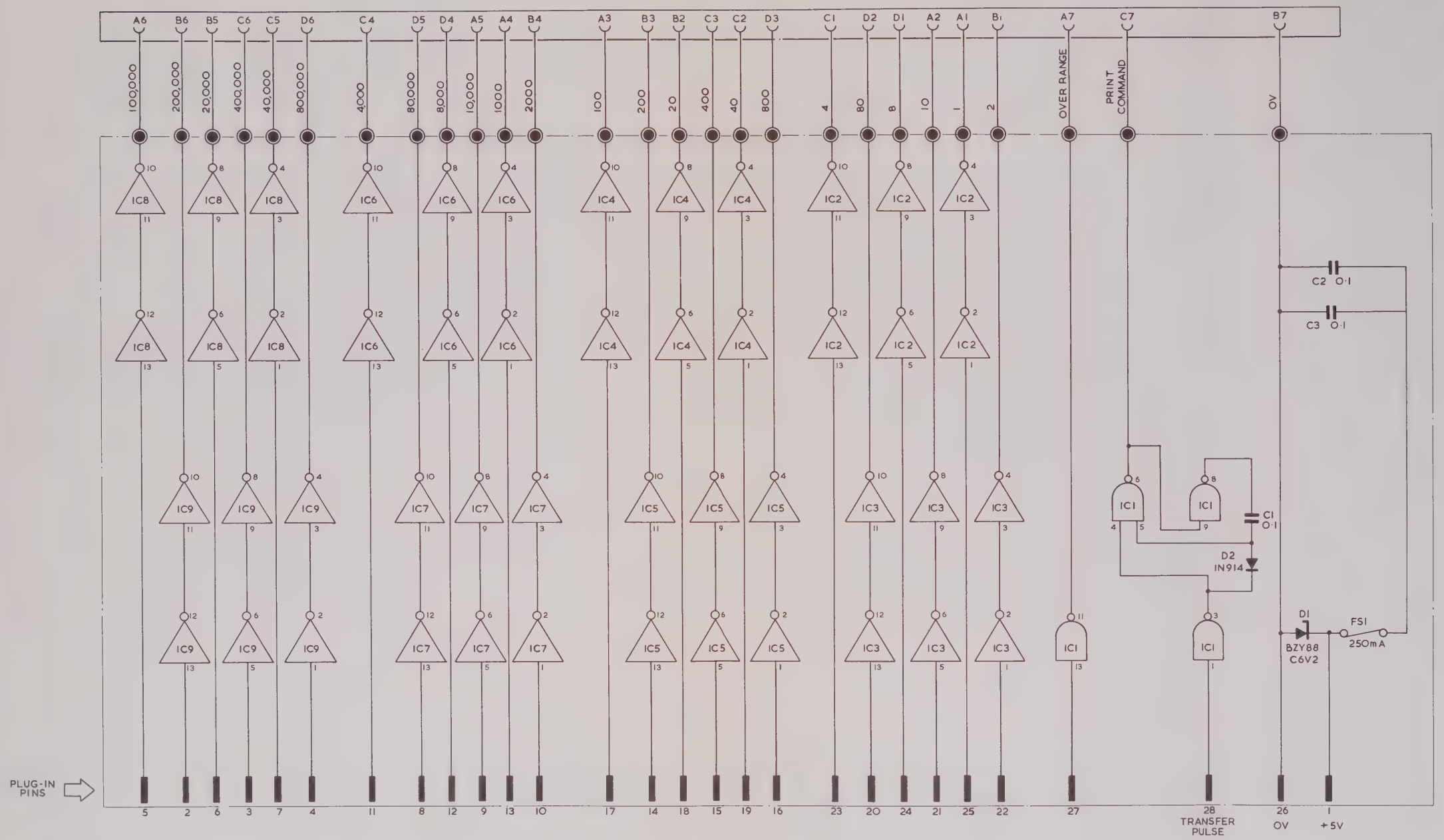


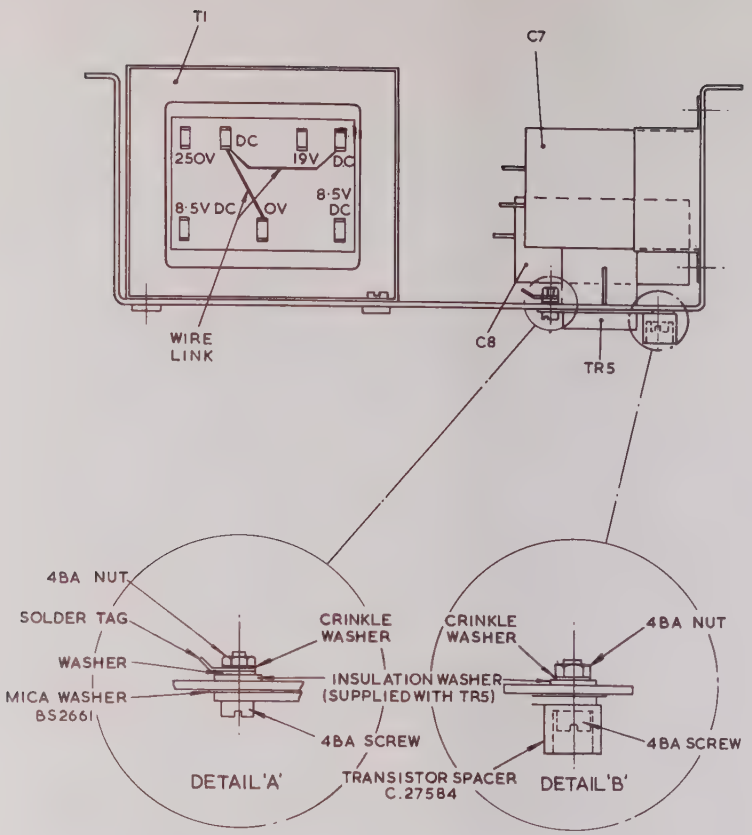
FIG. 7 B.C.D. OUTPUT BOARD – COMPONENT LAYOUT D.31660/1

FIG.8 BCD OUTPUT BOARD
CIRCUIT DIAGRAM B31664/1

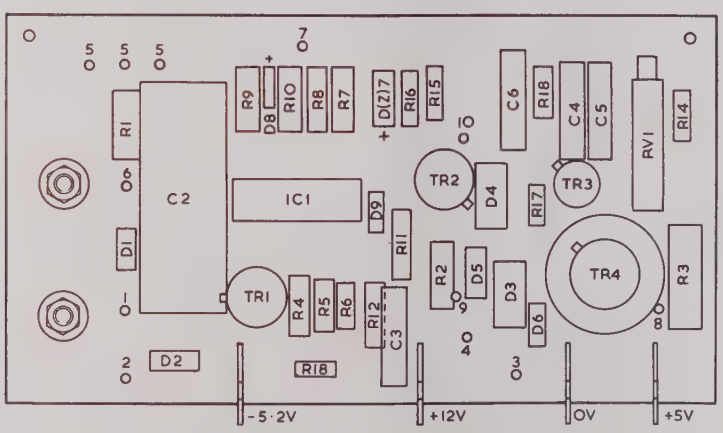


NOTES

1. SYMBOLS SHOWN THUS: ◉ INDICATE P.C. BOARD WIRING POINTS
2a. IC2 TO IC8 INCL. SN7404N PIN 7 0V, P14 + 5V
2b. IC1 SN7400N PIN 7 0V, PIN 14 + 5V

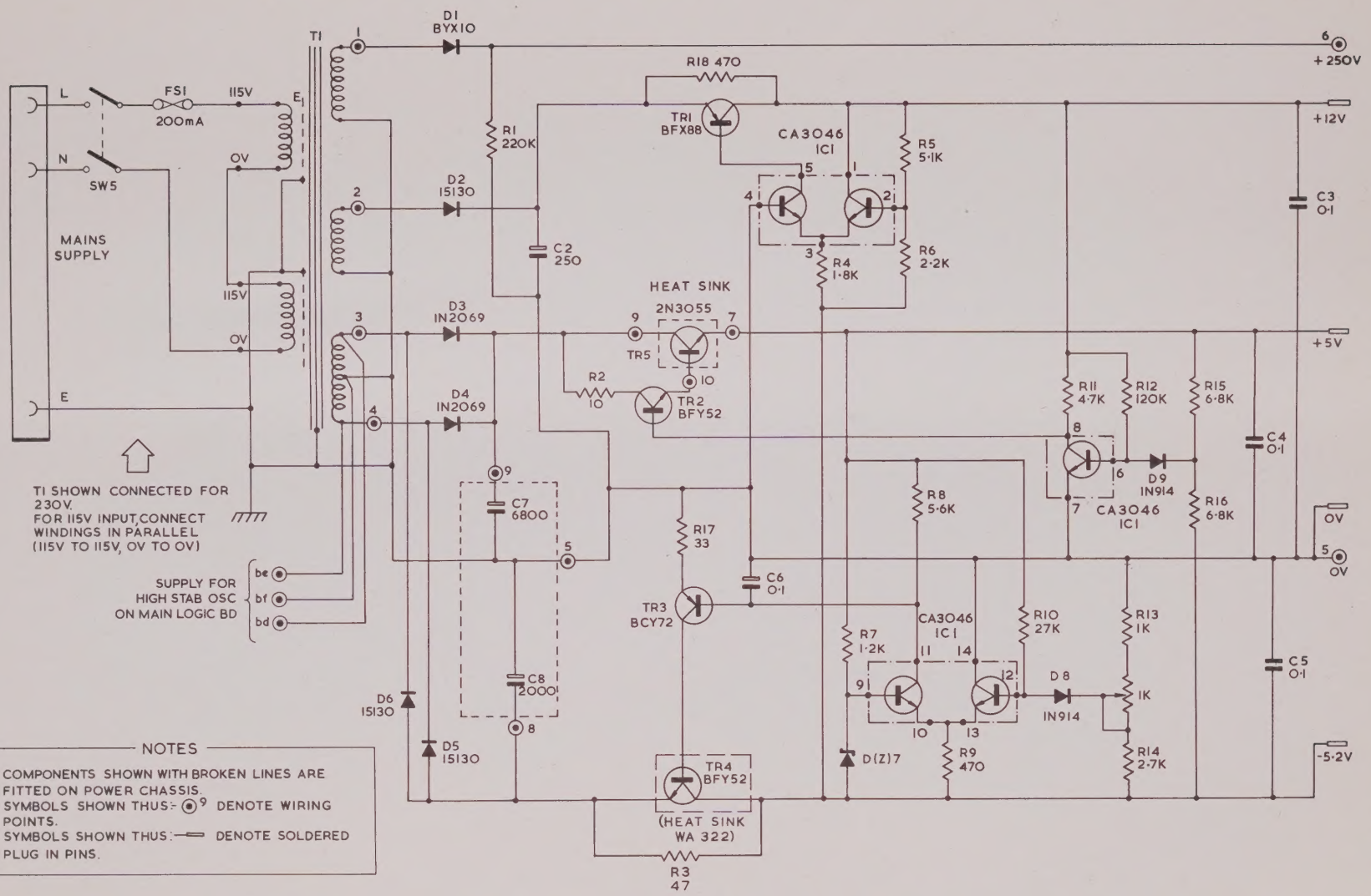


CHASSIS LAYOUT B.29701/2



BOARD LAYOUT D.29662/2

FIG.9 POWER SUPPLY UNIT - COMPONENT LAYOUTS



NOTES

1. COMPONENTS SHOWN WITH BROKEN LINES ARE FITTED ON POWER CHASSIS.
2. SYMBOLS SHOWN THUS:- ⊙9 DENOTE WIRING POINTS.
3. SYMBOLS SHOWN THUS:-═ DENOTE SOLDERED PLUG IN PINS.

FIG.10 POWER SUPPLY - CIRCUIT DIAGRAM B2691/2

MP MASTER
MA24014

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